Fermilab

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THE FERMILAB 200 MeV LINAC CONTROL SYSTEM HARDWARE

M. F. Shea

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CHAPTER 1

INTRODUCTION

This report is a description of the present Linac distributed control system that replaces the original Xerox computer and interface electronics with a network of 68000-based stations. In addition to replacing the obsolete Xerox equipment, goals set for the new system were to retain the fast response and interactive nature of the original system, to improve reliability, to ease maintenance, and to provide 15 Hz monitoring of all Linac parameters.

Our previous experience with microcomputer installations showed that small, stand-alone control systems are rather straightforward to implement and have been proven to be reliable in operation, even in the severe environment of the 750-keV preaccelerator. The overall design of the Linac system incorporates the concept of many relatively small, stand-alone control systems networked together using an intercomputer communication network. Each station retains its local control system character but takes advantage of the network to allow an operator to interact with the entire Linac from any local console. At the same time, a link to the central computer system allows Host computers to also access parameters in the Linac.

The individual local control stations are called Secondary stations and the system that controls the communication links to Hosts and Secondaries is known as the Primary. An overall view of the organization of the Linac control system is given in Figure 1.0.

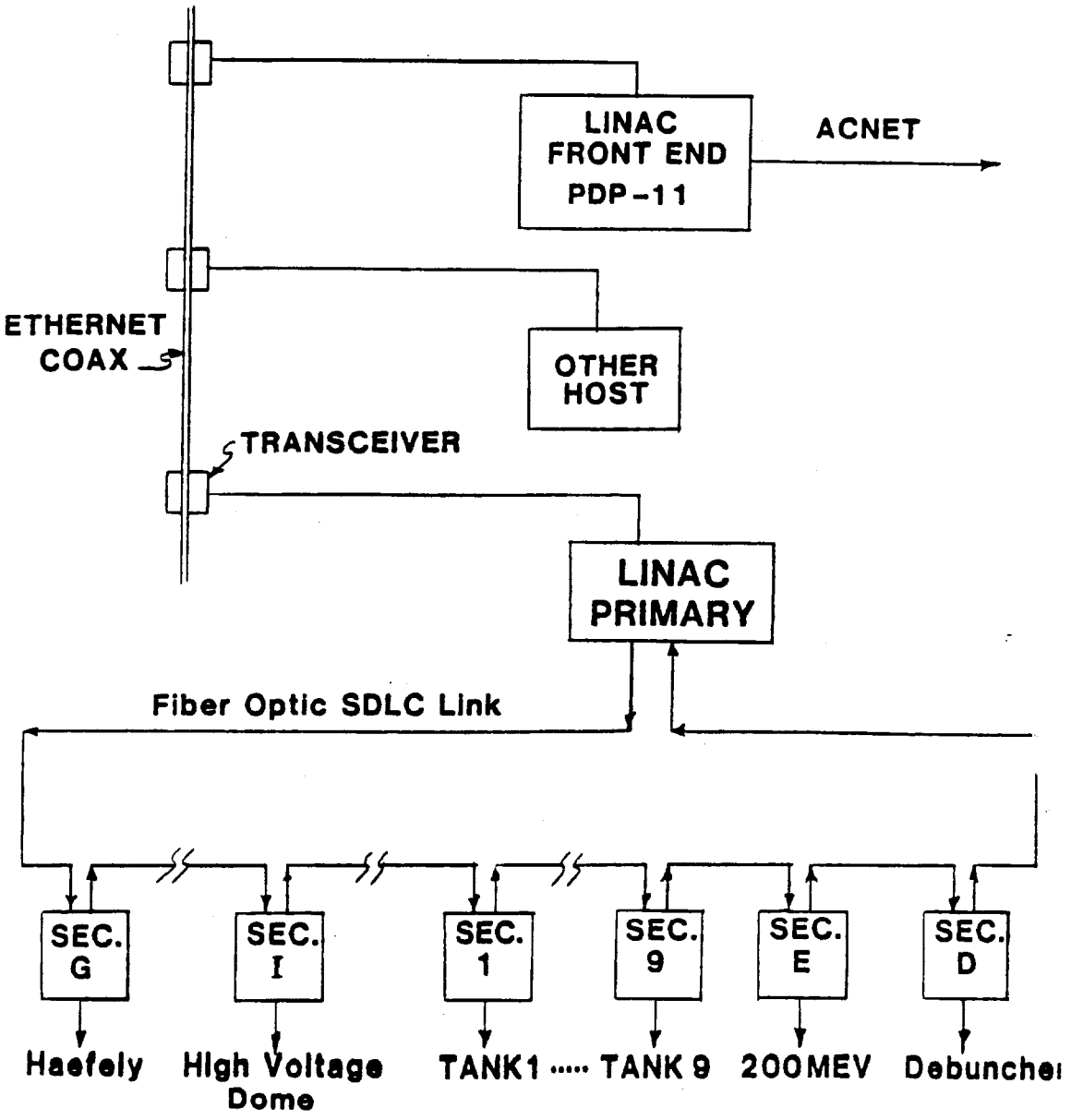


FIGURE 1.0 Organization of the Linac Control System

CHAPTER 2

ARCHITECTURE

2.1 INTRODUCTION

The Linac control system consists of seventeen stand-alone microcomputers interconnected using IBM's SDLC (Synchronous Data Link Control), a serial communication link protocol. Control stations are physically located so that each major equipment area has its own dedicated control station as shown in Figure 2.1. The communication protocol requires a Primary station to control the data transfers to the Secondary stations.

2.2 THE PRIMARY STATION

The Primary serves as the master station as defined by the SDLC Loop communication protocol and it also provides the connection between external Host computers and the Linac system as a whole. In its role as the SDLC primary, it initiates all message traffic on the link--- Secondaries may not initiate transmissions. On behalf of an external Host, the Primary will relay commands and settings to Secondaries, collect, sort and organize requested data and return it to the appropriate Host. The Primary operates synchronously with the Linac 15 Hz repetition rate.

2.3 THE SECONDARY STATION

Each Secondary station is, in effect, a complete, miniature control system. As shown in Figure 2.3.1, it contains all the essential elements of a real-time control system: a computer, analog input and output, binary input and output, and a complete console to allow operator interaction with the system. Figure 2.3.2 is a photograph of an installed Secondary showing the Multibus bin, the I² repeater, four A-D and two D-A chassis.

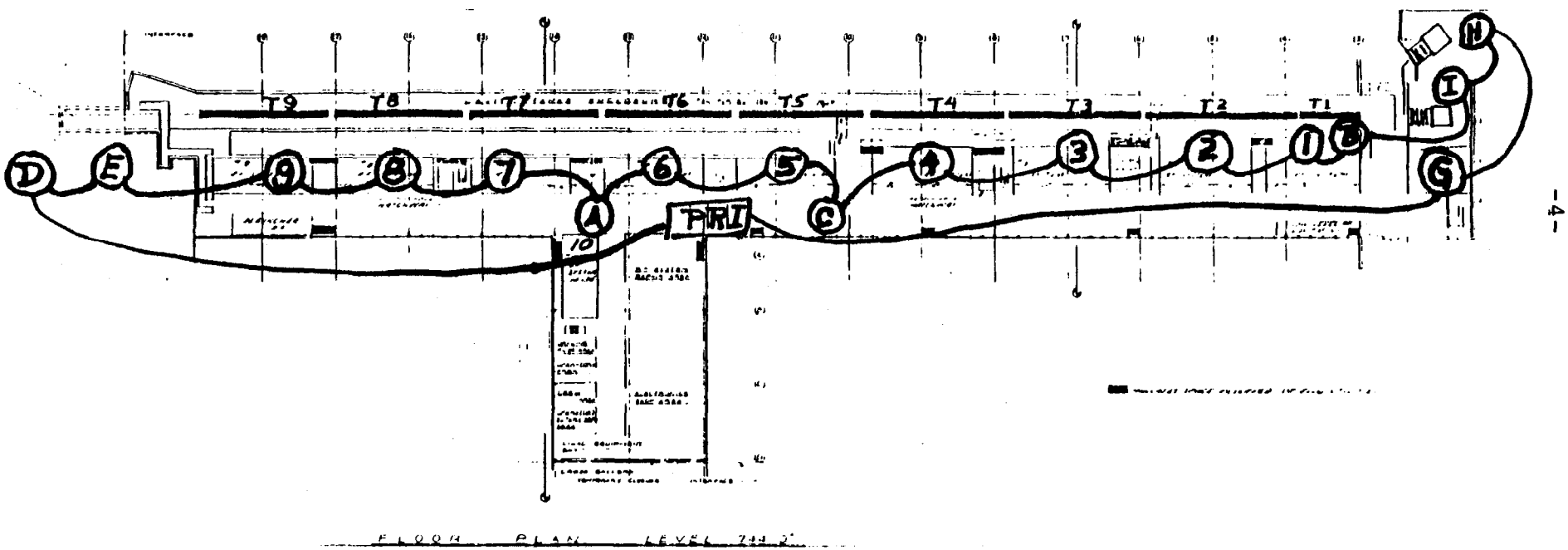


Figure 2.1 Location of Linac Secondaries

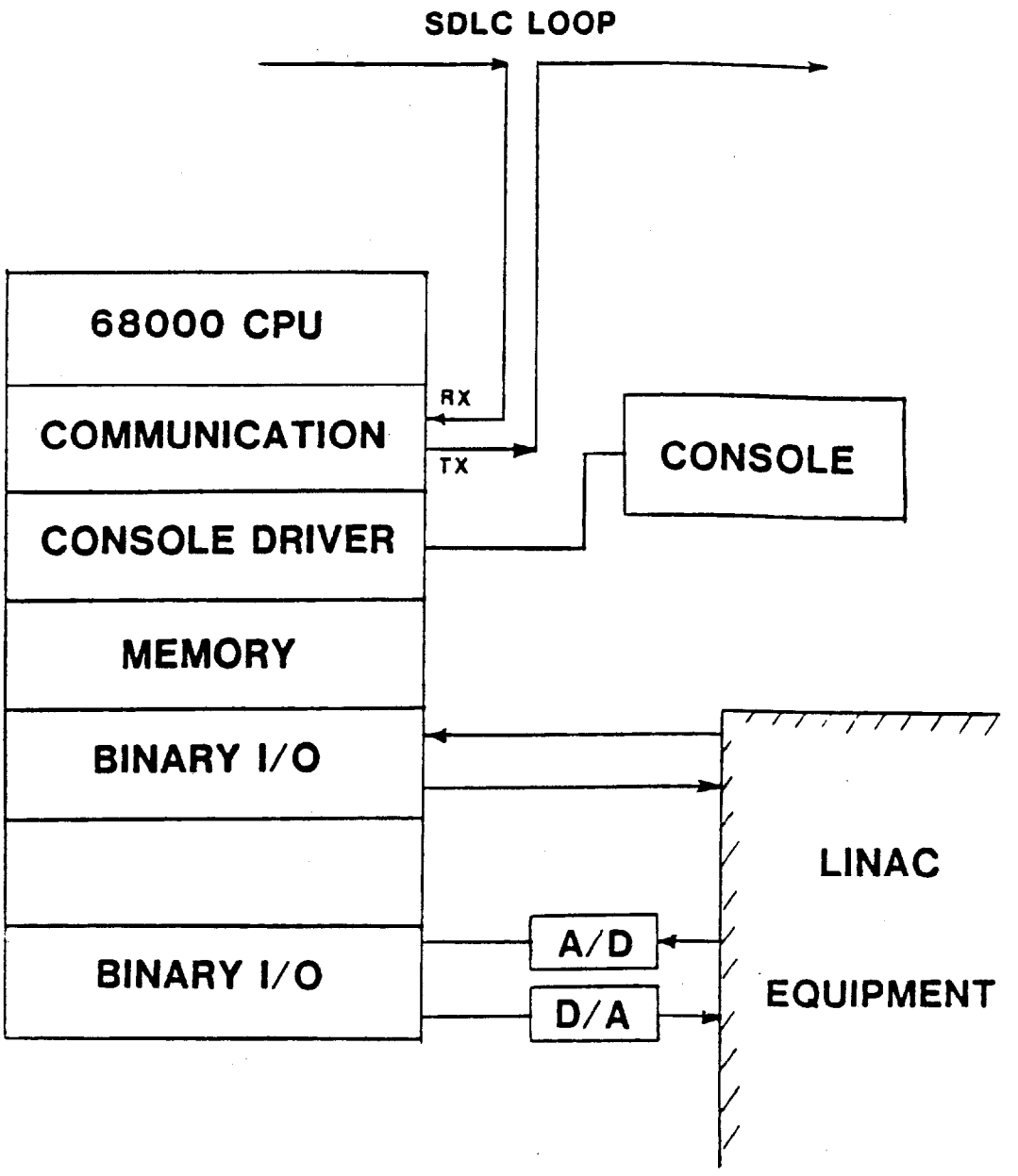


FIGURE 2.3.1 Block Diagram of Linac Secondary

FIGURE 2.3.2 PHOTOGRAPH OF SECONDARY STATION

The Secondary operates synchronously with the 15 Hz repetition rate of the Linac. Every 66 ms, the computer reads all the analog and binary parameters in its area, updates lists of data for requestors that need selected data from its area, performs the monitoring function to look for changes in alarm conditions, adjusts parameters that are under software closed loop control, executes the application program currently selected to run on behalf of the operator at the local console, updates the local console display as required, makes settings to local or remote parameters as requested, and handles all message-oriented communications that occur on the SDLC Loop. This sequence begins about beam time when the 15 Hz interrupt arrives.

All Secondaries receive their interrupt at the same time, so the activity described above is carried out in all Secondaries in parallel.

2.4 OPERATING MODES

Three distinct modes of operation are possible; the Local mode, the Global mode, and the Gateway mode. all Modes are supported simultaneously.

2.4.1 Local Mode

In the local mode, a Secondary can be used to control all the equipment for its own area. This is a stand-alone mode which implies that no other computers or communication links are required to operate. A local control console is an integral part of each Secondary, and from this console, the user can call up groups of parameters on a small video screen, observe the present values, and make changes to the analog and digital settings for the equipment in that area. An installed local console is shown in Figure 2.4.1. A local data base stored in non-volatile memory contains the names, titles, calibration constants, settings, nominal and tolerance values, and control characteristics of each analog and digital parameter in the local system.

Software in the local stations (Secondaries) consists of 1) a system part that performs the communications, interrupt handling, data acquisition, parameter monitoring, closed loop control, and console support; and 2) a selection of application programs that provide the operator's interface with the system. System programs are written in 68000 assembly language; the application programs are written in Pascal.

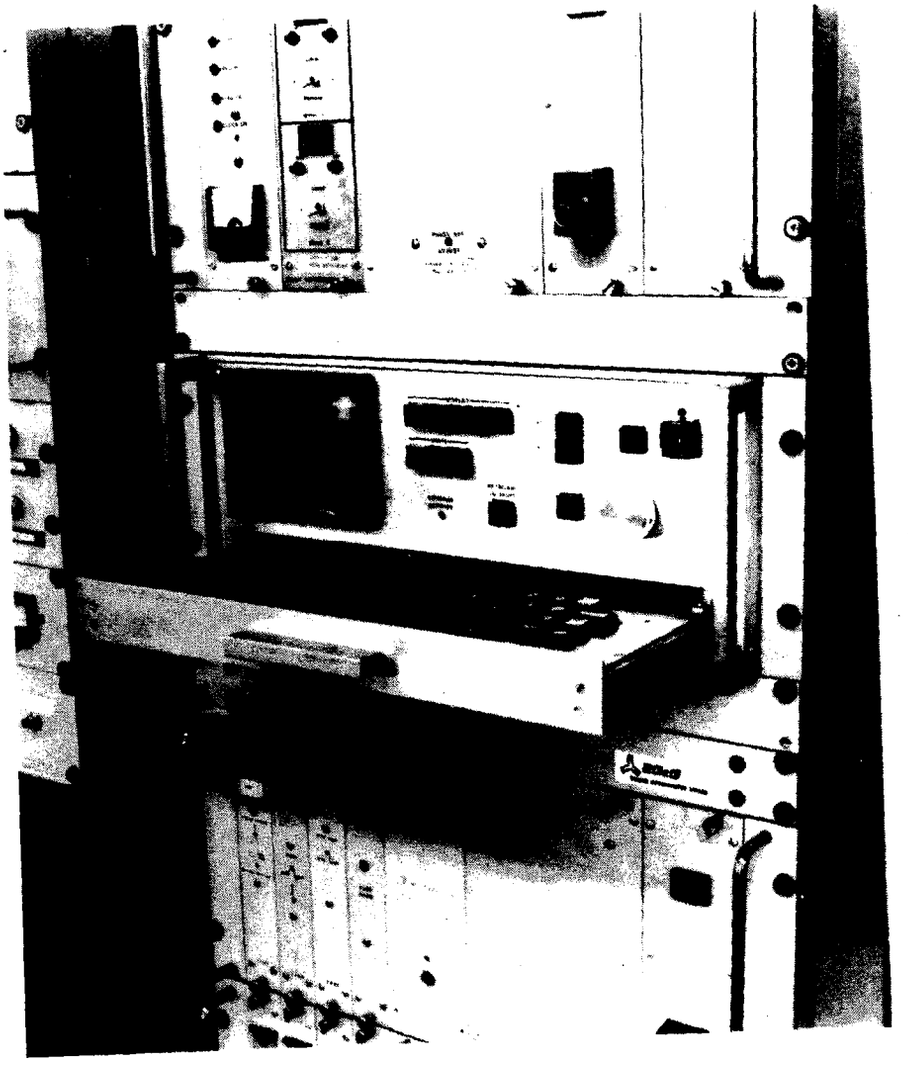


FIGURE 2.4.1 PHOTOGRAPH OF A LOCAL CONTROL CONSOLE

2.4.2 Global Mode

The global mode includes all the capability of the local mode along with the additional features of the Linac system that are available when the SDLC link is in operation. The net effect of the global mode is to allow an operator at any console to control and monitor any device in the entire Linac. This added capability is transparent to the user -- the same actions performed at a console will cause readings to be returned from (or settings to be made to) parameters in either local or remote locations. In this mode, ion source parameters may be adjusted by an operator using the console at, for example, Tank 3. From a single console, a technician can check the RF system parameters for each station without walking down the entire Linac gallery.

2.4.3 Gateway Mode

The Gateway Mode refers to the operation of the Linac system as a whole by way of the communication link that exists between the Primary and external Host computers. One Host, a PDP-11/34, serves as the Linac Front End computer for the central control system. A 68000-based Host, located in the Linac gallery, provides automatic, daily operational summaries for Linac and Controls group support personnel. Communication between the Hosts and the Primary is by way of Ethernet, a 10 megabit serial protocol that is now an international Local Area Network standard.

Using the appropriate messages, a Host can request and receive Linac data, and make settings to Linac devices. When a data request is received from a Host, the Ethernet address of the Host is remembered by the Primary so that the answer messages may be returned to the appropriate Ethernet Host address. Gateway accessing of the Linac system does not interfere with Local or Global Mode activity.

CHAPTER 3

OVERVIEW OF HARDWARE COMPONENTS

3.1 INTRODUCTION

The Linac stations consist of a microcomputer based in Multibus/IEEE-796 hardware, connected to a number of I/O cards and external chassis. The bins and power supplies are standard 12 slot Intel ICS-80 products and the board complement for a typical Secondary is:

1- Motorola MC68000-based CPU board
1- Communication board
1- 32K byte core memory
1- 9-channel predet timer
2- Binary I/O card

Slot assignments for a typical Secondary are as follows:

Slot 1- 9-Channel Predet Timer
Slot 2- Binary I/O (for normal binary control and sense)
Slot 3- Binary I/O (A/D, D/A, and OPTO22)
Slot 4-
Slot 5-
Slot 6-
Slot 7-
Slot 8-
Slot 9- 32K Core Memory
Slot 10-(not available- used by 32K Core Board)
Slot 11-Communication Controller
Slot 12-68000 CPU Card

Slots 4-8 are used for additional binary and analog I/O as required by individual Secondaries. Most of the AD/DA converters and the SDLC link repeater chassis are external to the Multibus bin. Each of the hardware components will be briefly described below. More complete descriptions for the boards are given in the Appendices.

3.2 THE MICROCOMPUTER

The CPU card and core memory card form the microcomputer that operates the Secondary station.

3.2.1 The CPU Board

Each Secondary is controlled by a 68000-based single board computer located in slot 12, the rightmost slot of the ICS-80 chassis. This computer is a Fermilab design because it was needed before commercial boards became available. General features of the board are:

8MHz 68000 CPU
8 pairs of 24 pin memory sockets
20-bit addressing
2 RS-232 Serial I/O ports
4 Bytes of parallel I/O
3 16-bit timers
Multibus/IEEE-796 compatible
Programmable memory addressing

The CPU card is currently configured to use 6 pairs of onboard memory sockets for program storage and two pairs for onboard scratchpad RAM. All Secondary programs reside in onboard ROM so the computer does not need to use the backplane for accessing instructions, but only for data and I/O transfers. No programs are downloaded and executed. The ROM sockets are all configured for 8K byte parts (96KB total) and the RAM sockets are for 2K byte parts (8K bytes total). Note that all Secondary CPU cards are identical -- including software. A CPU card from any Secondary can replace the CPU card in any other Secondary. Differences between systems are accomodated in data tables in the offboard non-volatile RAM board.

All the onboard I/O facilities are brought out to the annunciator panel to the right of the CPU board. Two bytes of input and two bytes of output are used for option switch inputs and LED indicators, respectively. The serial I/O ports are terminated in standard RS232 25 socket "D" connectors.

A small RESET button is provided on the CPU board, but the large RESET switch on the ICS-80 chassis may also be used.

Timers on the CPU card are not brought off the board. These timers are used for internal housekeeping functions by the system.

A complete description of the CPU card is given in Appendix A.

3.2.2 Non-volatile RAM Board

A 32K magnetic core memory board is used in most of the Secondaries (a CMOS RAM card may also be used). This is a commercially available card (Micro-Memory Model 8086) that occupies two slots in the Multibus bin. All fixed data specific to a given station resides in this memory, and therefore these cards are not directly interchangeable between Secondaries. The contents must be downloaded from the VAX. A single toggle switch, accessable from the front, activates the memory protect feature that disallows writing data into a preselected portion of the memory. Currently, the first 12K bytes are write-protected.

The 32K core board is the only Multibus memory in a Secondary station. It contains fixed data tables and the local data base information in the first 12K bytes. The remaining space is used for readings, settings, nominal and tolerance values and dynamically allocated communication buffers. SDLC communication messages are transmitted from and received into this memory under DMA control.

It is the non-volatile property of this memory board that allows a Secondary to operate stand-alone and to come up after a power outage in an operating state without the need to download information from another computer. During initialization following RESET, the most recent setting values for external parameters are sent to the hardware.

3.3 INTERNAL I/O BOARDS

The space available in the Multibus chassis is not sufficient to house all the I/O requirements for most Secondary stations. Communications cards, binary I/O and predet timers are Multibus cards and are included in the chassis. Analog I/O is placed in external chassis controlled by a Multibus binary I/O board.

3.3.1 Communication Card

A single Multibus card provides the communication I/O for each Secondary station. This card controls the console serial I/O, houses the video RAM for the console display and interfaces the Secondary to the Link Repeater chassis.

The local console is driven by asynchronous serial protocol like an RS232 terminal using a Motorola MC6850 ACIA. Each fifteenth of a second, two bytes of data are transmitted to the terminal to light the appropriate indicator lamps, and four bytes are read to acquire the pushbutton switch status, the keyboard data, and the shaft encoder knob reading. These serial signals are interfaced to the ACIA using opto-isolators to minimize ground loops between the computer and the remote terminal.

A composite video signal generated on the communication board is sent to the 5 inch monitor in the console, and an independent video output is available on a Lemo connector to use for an auxiliary display. The 32 character by 16 line display is generated using an MC6847 video display controller circuit. The display memory is in the memory space of the 68000 processor so data may be updated by simply storing ASCII data in RAM. An entire screen of information may be written in less than one vertical scan time. For flicker free operation, the program changes data only during the horizontal flyback time. Four characters are updated at the end of each 64 microsecond horizontal scan time. (~0.5 Megabaud) Limited graphics capability is supported by the 6847 controller and this allows some parameter and time plotting to be done from the local console.

The majority of space on the communications board is dedicated to the SDLC/DMA circuitry. A Motorola 6854 chip is the protocol interface to the serial link. It connects to the serial link chassis by a 26-conductor ribbon cable that carries the serial transmit/receive clocks and data along with several additional control signals intended to bypass the Secondary for several failure modes.

One megahertz serial data is received by the 6854 and automatically transferred to a 16-byte FIFO memory from where it is normally placed in memory under DMA control. The purpose of the FIFO is to allow some buffering time to prevent receiver overrun in case the DMA controller cannot immediately access the Multibus. Data to be transmitted is handled in a similar way and is stored in a transmit FIFO by the DMA controller and automatically transfered to the 6854 to be sent out serially on the SDLC link.

Interrupts generated by the SDLC and DMA controller chips are connected to Interrupt Priority Level 6 on the 68000 processor. This is the highest active level so that link interrupts may be processed quickly.

A more detailed description of the communication board is given in Appendix B.

3.3.2 Binary I/O

The binary I/O provided by the Xerox control system was organized as full bytes of output and full bytes of input. Each byte was cabled to the end rack in the control area and connected to the field wiring using AMP terminal blocks. To replace the Xerox equipment, a simple Multibus binary board was designed that provided for nine bytes of binary I/O. These signals are tied directly to the original Xerox cables. A typical RF station requires only seven bytes of binary I/O.

The binary card appears as nine bytes of memory in the I/O space of the 68000, so the binary data is handled with normal MOVE instructions. The card is constructed so each byte may be latched, and the output of the latch goes to both the 74XX output buffers and to the input of tristate buffers that allow the computer to read the stored data. To configure the byte for input, the latch is removed, and the output buffers are replaced by pull-up resistors. The tristate buffer then reads the state of the input lines. The binary I/O board receives only a power on Reset. Normal Resets do not change the stored values being output to the hardware. Although commercial Multibus boards are available with nine bytes of binary I/O, these designs use LSI interface chips that output both states during initialization. This is unacceptable for a system that is to control hardware (like vacuum valves)

To accomodate the need for stepping motor pulses (short ~20 microsec) and longer (fraction of a sec) pulses, the Secondary software forms the pulse by driving the selected bit to the active state and later returning it to the inactive state.

High power binary output and optically isolated binary inputs are achieved using OPTO22 devices. Each station has one byte of OPTO22 output and one byte of OPTO22 input.

The nine bytes of binary signals are grouped into 3 connectors each containing three bytes of signals. The 50 conductor ribbon cables interface the 24 bits to external equipment. Alternate conductors are grounded. Fused +5V power may be optionally brought off the board to power external devices (such as OPTO22 boards).

Secondaries normally have two binary I/O boards; one for normal binary interface and a second that connects to the OPTO22, the external A/D chassis and the external D/A chassis. Details of the binary I/O board are in Appendix C.

3.3.3 Predet Timers

Each Secondary has a Multibus compatible predet timer board that can output nine independent timing pulses. Each pulse is usually referenced to TZERO, the beginning of the Booster cycle, although jumpers on the board allow one timer to be triggered by the delayed output of the previous(or any other) timer. A 1MHz signal derived from the Booster clock is doubled by an onboard phase locked loop to form the 2MHz time base used by all timing channels.

Each of the 9 timers (known as timer 0,1...8) can have a resolution of 0.5 microsec and a maximum delay setting of 16384 microsec. Timers 2, 5, and 8 have a divide-by-eight prescaler that can be enabled to allow delays that cover the full 66 ms at a reduced resolution of 4 microsec.

These predet timers use Motorola 6840 chips. The output pulse width is set to 1 microsecond, and it is buffered off the board with a transformer coupled driver that can drive a terminated 50 ohm cable.

A watchdog timer included on the board is activated during the initialization sequence by the 68000. This timer is simply a retriggerable one-shot that is set for about 150 ms. During the execution of a task triggered by the 15 Hz interrupt routine, the 68000 addresses a register location on the timer board causing the watchdog timer to be retriggered. Failure to address that particular register will allow the one-shot to time out causing the watchdog timer circuit to generate a system RESET.

In normal operation, the watchdog timer should never time out. Failure modes that can cause a watchdog timer reset are: loss of 15 Hz clock, a bus error that causes the processor to halt, or any occurance that keeps the processor at an interrupt level so that it does not perform its normal tasks. Note that tasks are executed at the lowest level.

3.3.4 Multibus Analog I/O

Most of the analog I/O for a Secondary station is external to the Multibus bin. The exceptions are: areas that require bipolar D/A converters and the A/D and D/A converters in the H and I high voltage domes. Multibus compatible analog interface is used in the preaccelerators to allow these cards to be located in the shielded enclosure with the microcomputer. Using a large NEMA enclosure provides enough shielding to allow the system to survive arc-down of the HV terminal without interruption.

The D/A board is a commercially available 8-channel, 12-bit, bipolar unit (Datel Model ST800 DA). Internal D/As are used in systems 7 ,E ,G ,H ,and I. The A/D board is a single ended 32-channel, 12-bit, +10V to -10V MADC (Datel Model ST800 S32) .A/D converters in all other systems are external to the Multibus bin.

3.4 EXTERNAL I/O COMPONENTS

A typical Linac station supports 64 analog input channels and 16 D/A output channels. The present limit for a Secondary is 128 analog channels. For several reasons it is desirable to keep the A/D channels external to the Multibus bin: 1. Concentrating the analog cabling to Multibus cards is difficult, 2. Some Secondaries have insufficient space in the bin, 3. An external chassis is an electrically quieter environment for analog signals, 4. For trouble shooting and maintainence it is easier to swap out an external chassis than to replace an internal Multibus card. In any case, the amount of data transfers to I/O devices is much less than, for example, to memory cards, so a simpler, lower speed interconnecting scheme is adequate. Other I/O equipment is located external to the Multibus bin for reasons of physical placement and independent power.

3.4.1 The Local Console

A local console is included as an integral part of each Secondary station. It is normally within 20 meters of the Multibus bin, but longer distances are possible. Three coaxial cables interconnect the console and the Multibus communication board that drives it--- a transmit , a receive, and a composite video cable. The serial TX/RX cables carry 4800 baud data, and the composite video signal drives the 5 inch TV monitor in the console.

General features of the console are: a 16X32 alphanumeric display, a shaft encoder knob, a 64 key keyboard and 13 illuminated momentary pushbuttons. The lights are controlled entirely by the computer-- only the lights that are appropriate for the currently active application program will be operative. A key operated switch can disallow making settings from the local console although parameters may still be displayed normally. Details of the console hardware are given in Appendix D.

3.4.2 Fiber Optic Link Repeater Chassis

Data transmitted around the SDLC loop is carried on fiber optic medium chosen for its noise immunity and ease of incorporating stations H and I (the High Voltage domes) into the Linac system.

The fiber optic loop begins at the Primary located in Area 6, connects to G, the preaccelerator ground station and then goes to the H and I dome systems before going to B, the buncher system, and on down the rest of the Linac stations , to the 200 MeV area, and to "D" the Debuncher and back to the Primary. At each station, the data on the link is received and retransmitted by an external Fiber Optic Link Repeater chassis shown in Figure 3.4.2. Clock and data signals are encoded as a single Manchester signal so that only one fiber is needed. At each station the the light signal is received, decoded, and sent to the communications card. Transmit data from the communication card is sent back to the Repeater chassis to be encoded and sent to th next station.

Repeater functions are separately powered chassis so that Secondary stations can be powered down without interrupting the link traffic. Provision is made to Bypass the local station in order to maintain the integrity of the SDLC loop, even if a problem exists in individual Secondaries. The Repeater may be switched into Bypass manually, under program control, power loss in the Secondary station, or if the 26-conductor interconnecting cable is unplugged.

In the Bypass mode, the Repeater will decode and re-encode the data it receives and transmit it to the next station. Although the decoded data is still sent to the communication board, the 68000 will not act upon any received message if the station is off-loop.

Each repeater recovers the encoded clock from the received data, and this clock is used for transmitting. Another clock is built into each Repeater for use when a "beacon" message is transmitted. According to SDLC Loop protocol, a station should receive flag characters when no messages are present. If a station does not receive flags, it must transmit a special Beacon message that includes its own address to aid in locating the link problem. The Secondary will enable its own local clock to use if the upstream link has failed. In normal operation, only the Primary uses its local clock. All other stations recover the clock from the incoming signal.

Details of the Repeater chassis are in Appendix E.

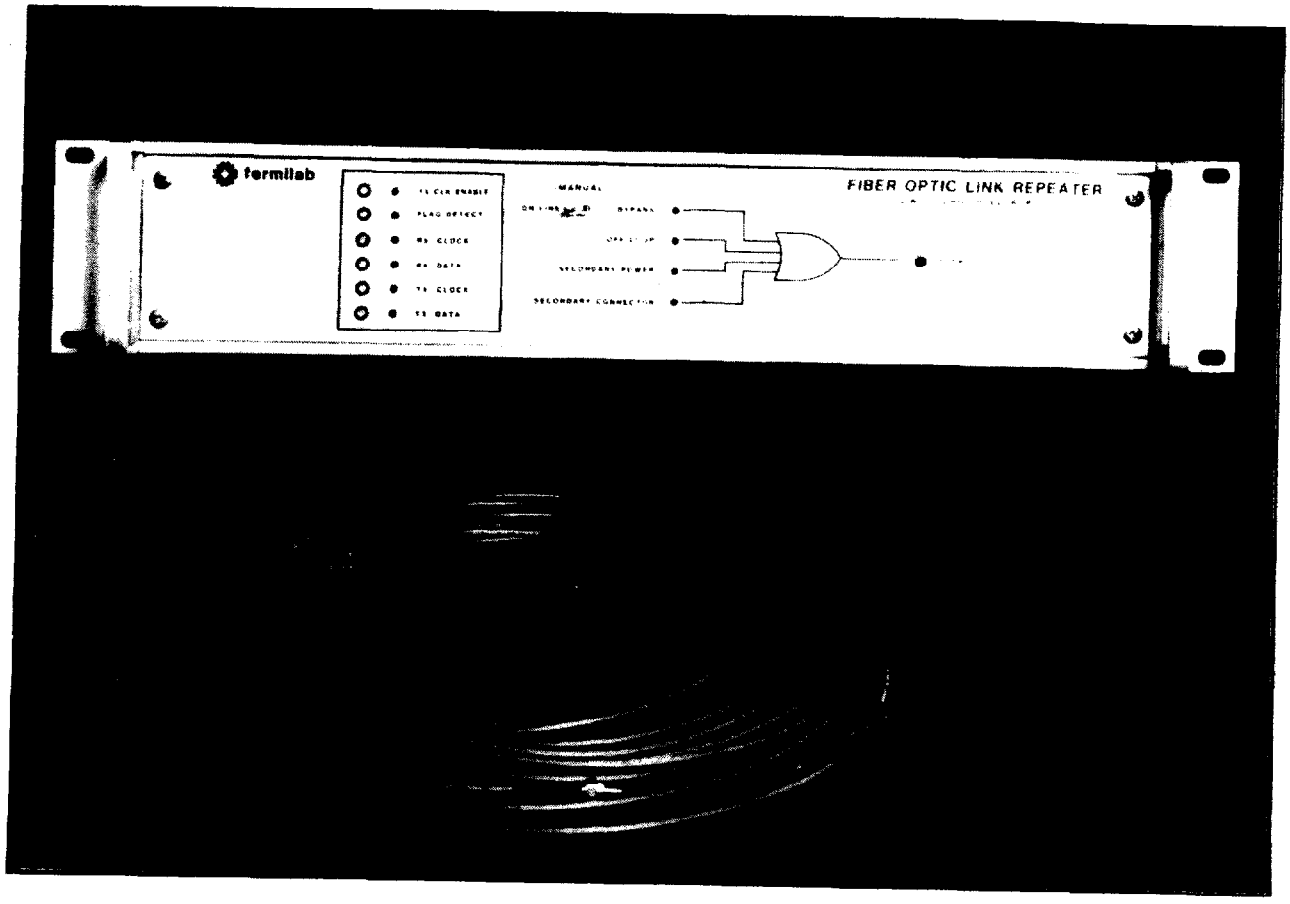


FIGURE 3.4.2 PHOTOGRAPH OF REPEATER CHASSIS

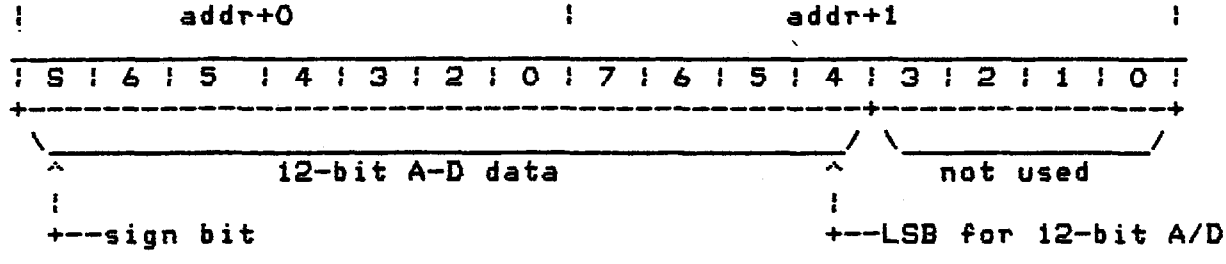
3.4.3 OPTO22 Binary I/O

Some of the binary I/O signals require higher drive outputs or isolation from local grounds. A 16-channel OPTO22 mounting rack is located at each Secondary--- one byte for input and one byte for output. Typical signals interfaced to the OPTO22 devices are: beam inhibit, RF reset, RF enable, and quad reset outputs and beam cycle input bit.

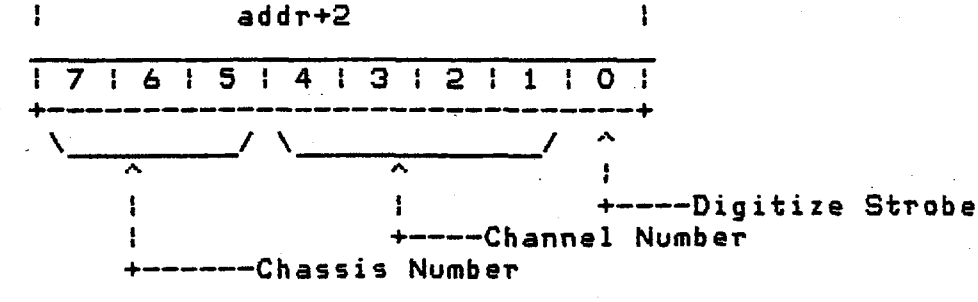
3.4.4 Sample-and-Hold / A-D Converters

Nearly all Linac signals are pulsed and need to be sample-and-held before digitizing. A combined 16-channel S-H / A-D was developed for use throughout the Linac. Signals are input on two 8-contact Burndy coax connectors to individual S-H amplifiers, and the held outputs are input to a 16-channel, 12 bit MADC module. Each Secondary (except H and I) has 3 to 5 such chassis. A single trigger causes all signals to be held simultaneously, and all chassis are normally triggered at one time using the Linac TDATA pulse.

The S-H/A-D chassis are driven by a single 50-conductor ribbon cable using one of the three-byte interface connectors on the binary I/O card. The three bytes are used as shown below. Figure 3.4.4 is a photograph of the A-D chassis.



(A) A-D DATA BYTES



(B) A-D COMMAND BYTE

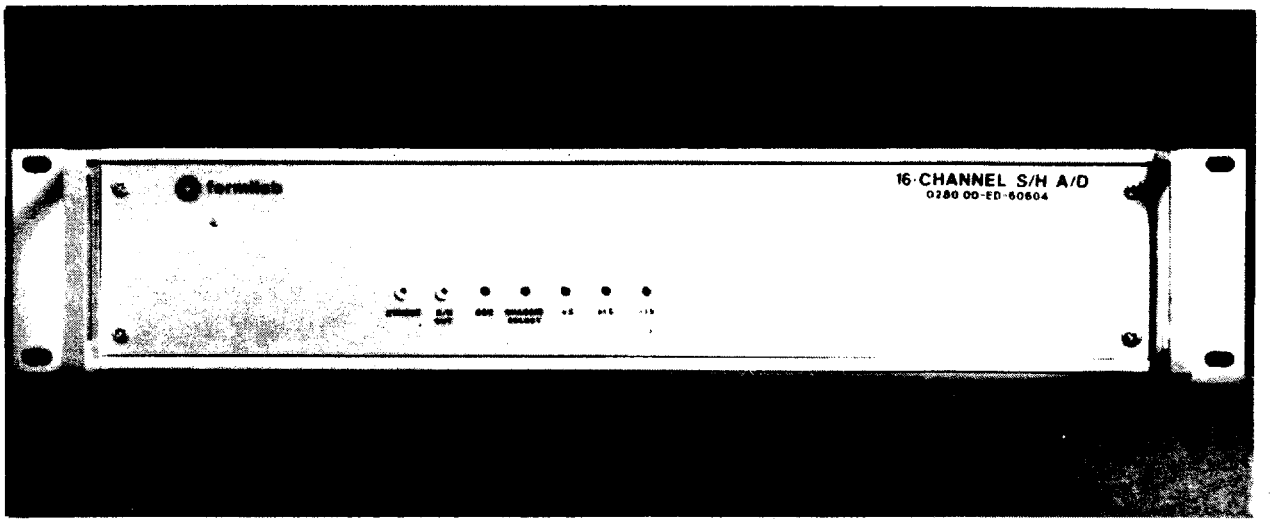


FIGURE 3.4.4 PHOTOGRAPH OF 16 CHANNEL S/H A/D CONVERTER

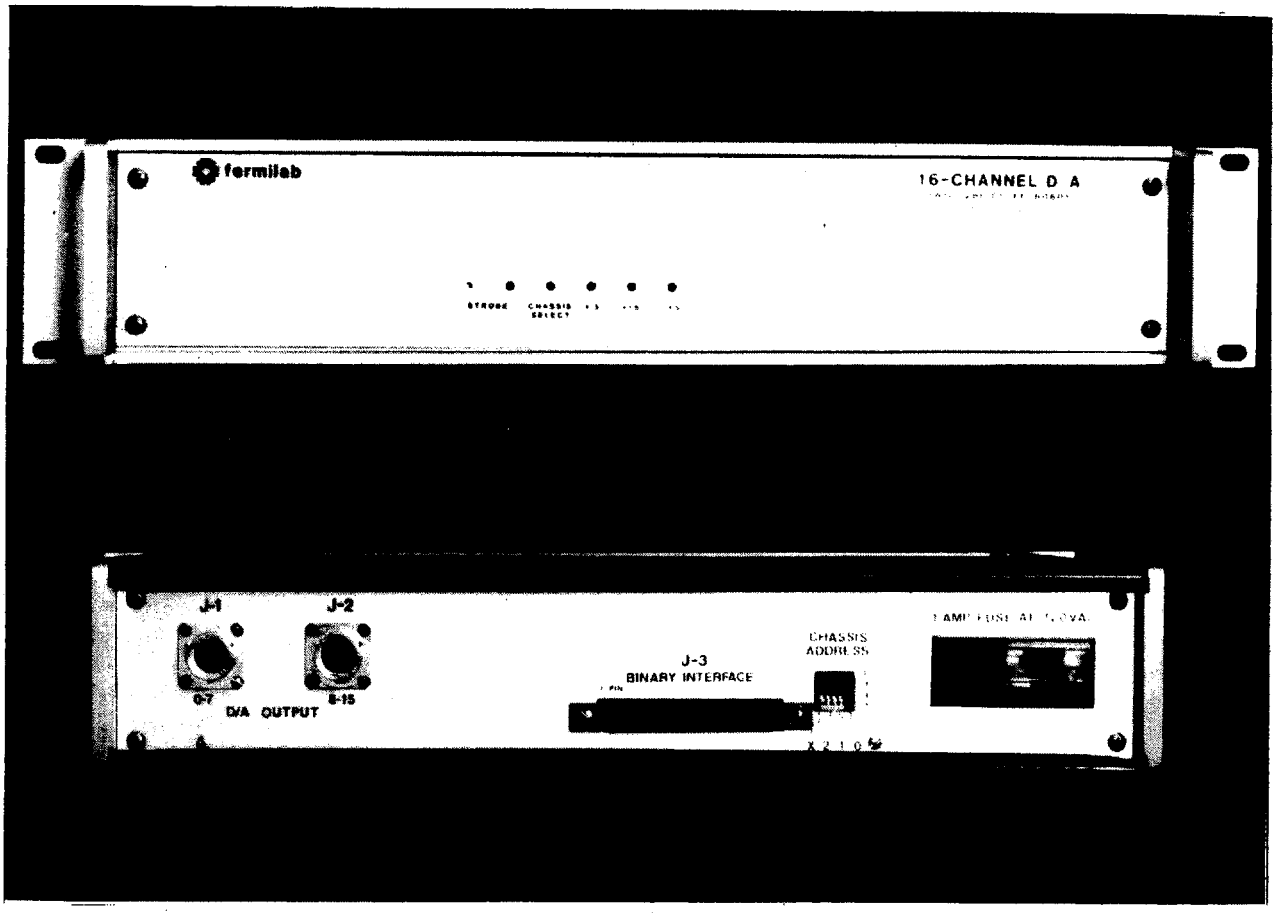


FIGURE 3.4.5 PHOTOGRAPH OF 16 CHANNEL D/A CONVERTER

Note that data are returned left justified in a 16-bit twos-complement word and therefore higher or lower resolution A-D converters could be used for more or less precise measurements. In the data returned by the twelve-bit digitizers, the 4-bit channel number is returned in the four least significant bits of the 16-bit word.

The least significant bit of the command byte is a software-generated "digitize" strobe, and the remaining bits select both the channel number within the chassis and the chassis number. This allows the addressing of eight 16-channel digitizers or 128 analog channels. The chassis address switch is a DIP switch accessed through the rear pannel of the individual A-D chassis.

Using the addressing arrangement described, all the external A-D for a Secondary station are interfaced through a single daisy-chained 50-conductor ribbon cable that plugs into any of the 3-byte binary I/O connectors.

The normal MADC module (Analogic Model 6812) is set for +10V to -10V analog input range. In Secondary stations that control RF systems, the first A-D is configured for +2.5V to -2.5V full scale range in order to improve the resolution for the RF power level measurements. These signals are typically in the range of zero to one volt. A red label reading "FULL SCALE +-2.5 VOLTS" is located in the upper right of the front panel on these units. Details of the A-D chassis are given in Appendix F.

3.4.5 External D-A Converters

External 16-channel D-A converter chassis are located in most Secondary stations. They are used to set the reference level for the 171 Linac quadrupole power supplies and the low energy beam transport magnet power supplies. Analog output of these D-A chassis are 0-10 volts.

Sixteen integrated circuit D-A converters are housed in a chassis. Each D-A chip has onboard latches and outputs current to a buffer amplifier. The Secondary processor controls the D-A chassis in a manner similar to the A-D addressing discussed in Section 3.4.4, and the interface to the D-A chassis is the same, except that all three bytes of data are output; two for data and one for command. A photograph of the D-A chassis is shown in Figure 3.4.5. Details of the D-A chassis are given in Appendix G.

3.4.6 The MIL-1553 Interface

Because of the noisy electrical environment, a serial data transmission system has been implemented in the Preaccelerator Ground station area to interface the two Haefely high voltage generators. This serial protocol is military standard MIL-1553, a 1 MHz multiplexed bus that operates in a half duplex command/response mode. The bus itself is a shielded, twisted pair, multidrop arrangement that is transformer coupled, at each drop and at each station, to provide good electrical isolation between stations. Because it is a popular standard, at least in military circles, commercially available LSI chips are available to support the data transmission protocol.

On a MIL-1553 bus, each data transfer is initiated by the controller and received by a Remote Terminal (RT). The command is followed immediately by data if the RT is to receive information. After a delay of 4-12 microseconds, the RT sends a status word back to the controller. For a transmit command the controller sends only the command and the RT returns a status word followed by requested data. An attractive feature of the MIL-1553 standard is that the RT can be simple hardware; it may be, but is not necessarily, intelligent. The maximum total length of a MIL-1553 bus is determined by specified voltage limits at the transmitter and receiver, and by the required response time of the Remote Terminal. In practice, a MIL-1553 bus can reach anyplace on a big airplane; a few hundred feet.

All words in the MIL-1553 messages are 16-bit of data preceded by a 3-bit sync character and followed by a parity bit. The MIL-1553 system can be understood by examiming the command word in Figure 3.3.6. The command word consists of a 5-bit RT address, a 5-bit subaddress, a 5-bit word count, and a Transmit/Receive bit (T/R). The single word command can then address one of thirty-two RT's (actually only thirty-one are possible because RT=31 is used for broadcast commands). Within a selected RT, the controller can access one of thirty subaddresses and command it to receive or transmit up to 32 sixteen-bit words of data.

The command word establishes the general size of a MIL-1553 system; thirty-one RTs with thirty subaddresses each. Note that although each subaddress can transmit or receive up to 32 words, these words are only accessed sequentially and cannot be addressed individually or randomly. The characteristic of the MIL-1553 standard that the RT does not need to be a computer means that it can be as simple as hardware that strobes data into a latch, or enables status input data to be transmitted on the bus. It is the ease of connecting several devices in an area with a single twisted pair cable, that makes MIL-1553 an attractive standard for use in a control system.

The MIL-1553 specification defines the cabling, signal levels, termination and data protocols of this standard. It does not define the internal organization of the RT hardware beyond the connection to the bus; that is left to the system designers. The implementation chosen for the preaccelerator area uses Eurocard hardware interconnected with a simple bussed backplane. The RT electronics is contained on a single sized Eurocard (100 by 160 mm). This card provides the interface between the twisted pair MIL-1553 bus and the parallel backplane. Subaddresses within the RT are decoded on other single sized Eurocard function modules.

To control the Haefely high voltage set, only four interface cards are needed; a relay driver output card, two binary input cards and a stepping motor pulse serializer card. The Haefely is operated by actuating relays that parallel the local control panel push buttons and the digital status is read from contact closures of relays driven by the local control panel. An existing Haefely analog control module provides a 14-bit digital measurement of the high voltage terminal potential and this value is read into a binary input module. The reference voltage that determines the setting of the high voltage is generated by a D-A that is interfaced to appear as a stepping motor. That is, the computer can only send incremental up/down pulses to cause relative adjustments to the present value. This control is provided by a Eurocard module that receives a 16-bit word by a MIL-1553 command and counts the value to zero by counting up or down depending on the sign of the 16-bit word. Up/down pulses are output as CCW/CW pulse trains to the analog control module.

Physically the control electronics for each Haefely consists of a 5.25 inch by 19 inch rack-mounted Eurocard chassis containing a modular power supply, the MIL-1553 RT module and the four interface cards described above. Data that is accessed by a MIL-1553 connection has been made one of the data types recognized by a Secondary station. As with other allowed data types, this data is known to the system by entries in the data access table that resides in non-volatile core memory.

CHAPTER 4

TIMING SYSTEM FOR THE LINAC

4.1 INTRODUCTION

All Linac timing is derived from the Booster phase reversal clock. This bipolar clock is driven from the MAC room to relay rack LUO-RR1-3 in the preaccelerator area where it is received into a clock backup module and passed on for use by all Linac timers. From the clock backup module the clock signal goes to the H- and I- domes via fiber optic light pipes , to manual predet timers in the preaccelerator area and to a cable that supplies the Booster clock to all the Linac Secondary stations. A block diagram of the timing system is shown in Figure 4.1.

4.2 MANUAL PREDET TIMERS

Timing requirements for the Linac are rather modest. A fixed trigger is required for the pulsed quadrupole power supplies, the RF systems, and the 15-Hz interrupt for the Primary station. These fixed timing triggers are generated by a manual predet in the preaccelerator area. Settings of these triggers are seldom changed. In the upgrade of the Linac system, only the source of the triggers was changed--- the buffering and distribution of trigger signals along the Linac was left unchanged.

4.3 VARIABLE TIMING TRIGGERS

In the original Linac control system, the only computer controlled variable timer channel was TDATA, a pulse used to trigger all the sanple-and-hold amplifiers in the Linac. When the H- preaccelerator was installed, both the dome and H- ground station used local variable predets. In the present system, stations G, H, and I are operated using variable timers that are delayed from the Pulse Shifter output.

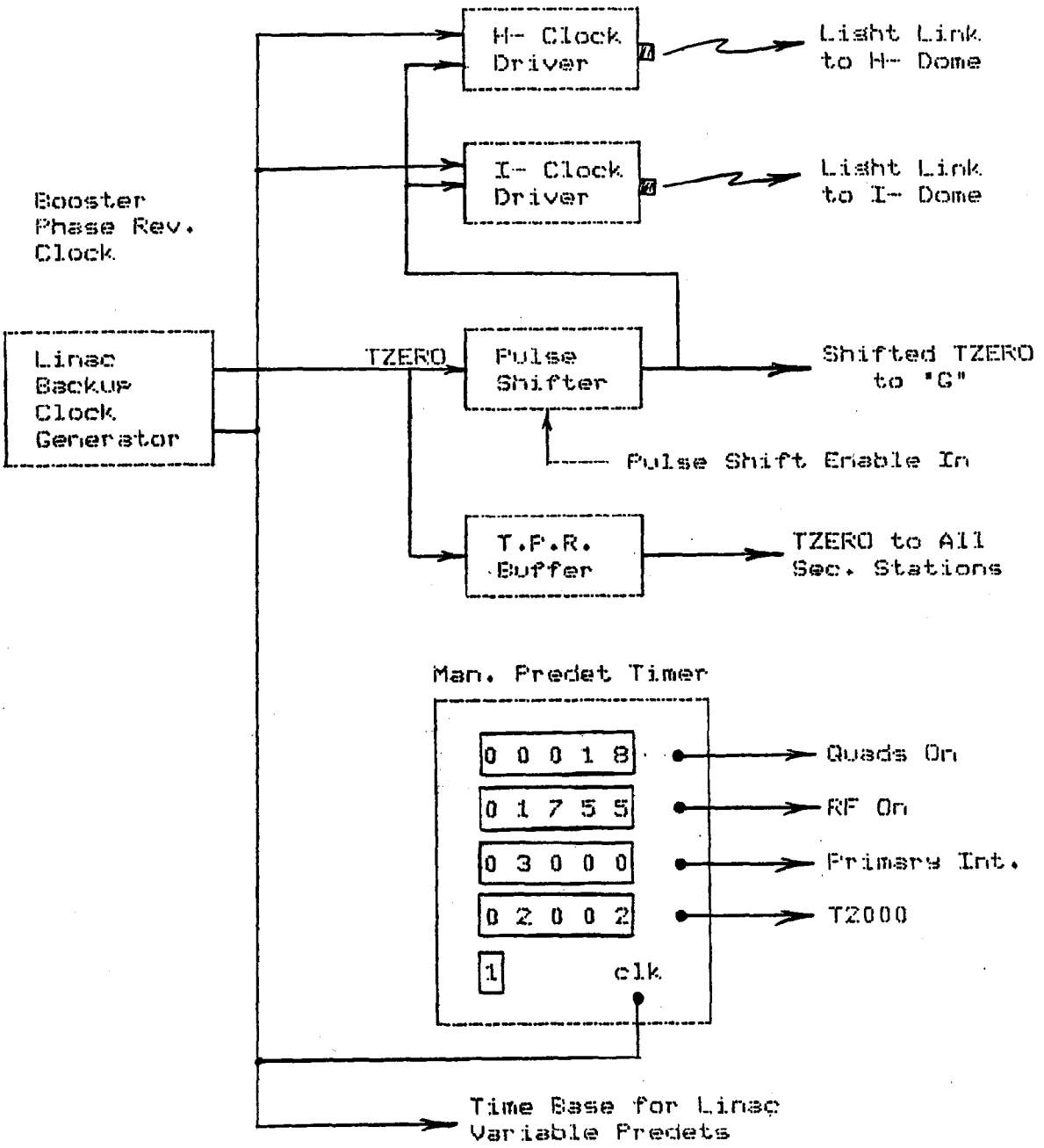


Figure 4.1 Block Diagram of Linac Timing System

4.3.3 Local Secondary Timers

Each Secondary is supplied with a programmable 9-channel timer board. One of these timers is used for the Secondary's own 15 Hz interrupt that determines when the processor reads its analog and digital data. Other channels, accessible from the back panel of the Multibus bin, are for local and future use.

4.4 NTF TIMING

A manual predet timer, triggered at TZERO time, is installed in the Neutron Therapy Facility. It provides the timing used in the 6800-based system that collects and accumulates the neutron dose data.

4.5 CLOCK BACKUP MODULE

The loss of 15Hz triggers is harmful for some Linac systems. Therefore, a clock backup module was developed to insure a continuous source of timing triggers in the absence of the Booster clock.

This module receives the Booster clock, decodes the phase reversals, regenerates the clock signal and outputs it as a normal bipolar clock. All phase reversals are transformed to single phase reversals so that manual predet timers can trigger continuously at 15 Hz by selecting a "1" on the digiswitch.

This module includes a 1 MHz crystal oscillator and a 15 Hz generator locked to the 60 Hz line. If either the phase reversals or the 1 MHz are lost, the backup module will continue to output a clock using its own internal generators. These operate independently so that if only the phase reversals are lost, the output clock will be the Booster 1MHz with the locally generated 15 Hz phase reversals.

It is intended that an additional clock backup module be placed in each high voltage dome to insure continuous triggers for the ion source in the event the clock from the ground station is lost.

This module also outputs a TTL-compatible 1 microsecond pulse at 15 Hz and a trigger that occurs for a three phase reversal event on beam cycles. For use in the domes, the backup module should encode its phase reversals at pulse-shifter-out time. The pulse shifter trigger is sent to the dome as missing pulses on the clock light pipe. Provision is made to input to the backup module, an external

trigger to be encoded as a phase reversal on the backup module's output. This feature will be used in the dome systems only, where the pulse shifter signal is input to make it the reference time for dome timers.

When the input clock to a backup module fails, the next output trigger will be delayed by at most one fifteenth of a second. No two phase reversals are allowed to occur closer than three line cycles (about 50ms). This eleminates the possibility of two closely spaced TZERO pulses when switching from internal to external clock.

CHAPTER 5

NEUTRON THERAPY FACILITY

5.1 INTRODUCTION

Because the Neutron therapy facility is a user of Linac beam, its controls are integrated into the Linac control system. The original 6800-based beam line microcomputer was left intact and interfaced to a normal Secondary station (Sec C). This Secondary receives data from, and makes settings to, both the 6800 system and its own analog and binary interface equipment.

5.2 THE NTF 6800 SYSTEMS

In 1975, a 6800-based system was put into operation to allow local control of the NTF facility. This system consists of two microcomputers; the Medical Control Room microcomputer and a Beam Line microcomputer interconnected by a byte serial FIFO link. The Beam Line system reads and integrates ion chamber data to provide dose accumulations for patient treatment and radiobiology studies. Because of the critical nature of the function it provides, considerable effort has gone into testing and verifying the operation of this system to insure its readings and calculations accurately record the actual dose the patient receives. We therefore decided to leave the 6800 system intact and simply connect it to Sec C in the same way it was interfaced to the Xerox 530. The NTF system is then essentially unchanged, except that its data is available to the new control system.

Originally, the Beam Line system had a second FIFO port to connect with the X530 and the Medical Control Room. The connection to the Medical Control Room is also the same, so the operation of the facility by the medical technicians is unchanged.

5.3 THE NTF SECONDARY

Secondary C, the NTF station operates as a normal Secondary. It contains all the functions and controls all the devices that pertain to the operation of NTF. Data acquisition is a combination of readings from Sec C's own analog and binary interface, plus data received from the Beam Line 6800 system. The choice of which system reads a given channel was made by simply accepting from the 6800, any data it is reading and interfacing all other channels directly to Sec C. In this way, there is exactly one reading of each parameter, and Sec C has a copy of the values being used internally by the 6800. In all other respects, Sec C is a normal station, so NTF data is available to any Linac Host or Secondary.

5.4 NTF TIMING

To provide a hardware source of interrupts for the 6800 Beam Line system, a manual predet timer is installed near the 6800. This timer is driven by a Booster clock from the MAC room and uses a TZERO trigger as its external referance. Two output pulses from this timer are used to provide the two interrupt triggers needed by the Beam Line system.

CHAPTER 6

OPERATIONAL CONSIDERATIONS

6.1 INTRODUCTION

A cursory check of the operation of the Linac system is available on the top line of most Linac programs on the control room consoles. There the operator will see a green character to indicate the station number of each secondary that responded to a test poll issued by the Primary. There are 30 possible secondaries but only 18 currently exist. They are numbered 1...9,A,B,C,D,E,G,H,I,V corresponding to Linac tanks 1 through 9, the test station (system 10), buncher, NTF(CTF), debuncher, 200MEV, preaccelerator ground station, H minus dome, I minus dome, and the primary console, respectively. A system that fails to respond will be replaced by a dot on these displays. If only dots appear on the top line when Linac application programs are called up, then the Linac Fron End PDP-11 is down or the Linac primary is down or the SDLC Link is not working.

6.2 STATUS OF THE PRIMARY

The Primary system is located in the controls area of Linac system 6. It is a dual - 68000 processor system; one processor is a dedicated link driver and the other drives both the Ethernet link to the Front End and its own console.

A small video screen above the primary is controlled by the Link Driver. Figure 6.2 is a copy of this display. Line 1 is the title, date and time. Line 4 is again the display of Secondaries that responded to the test poll. Line 3 shows the Secondary stations that are currently returning data to requestors. The requestor may be a Host like the Front End or a Secondary. If a Secondary is a requester receiving data, its position on line 3 will be displayed as inverse video (non blinking). On line 2, the numbers following the H: and L: are the numbers of active lists of data that are being collected by the Primary on behalf of the Host and the Linac stations. The time given on Line 2 shows when the Primary has finished collecting

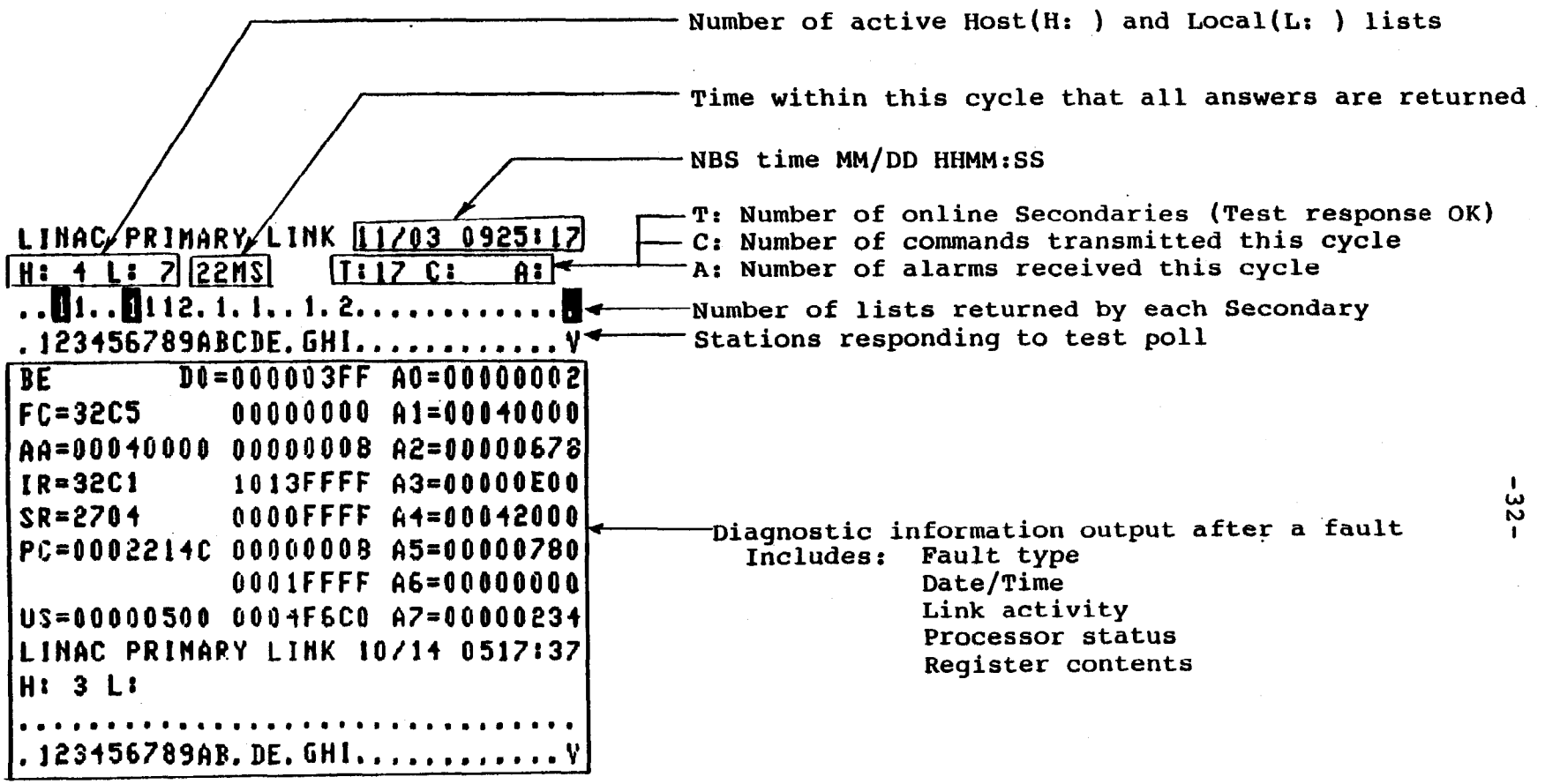


Figure 6.2 Status Display for Primary Station

data and has sent the last list of data to a requestor. The number displayed measures milliseconds from 15 Hz interrupt time. Currently, the Primary begins collecting data at ten ms into the cycle. The C: and A: give a count of the number of command and alarm messages that were serviced during the present Linac cycle.

If the Linac SDLC link is broken, then the next operating secondary will send a special "Beacon" message to the Primary. This feature of the SDLC Loop protocol is intended to help locate a link problem. Indication of a beacon message is shown by a station number on line 3 that is blinking between normal and inverse video. The problem then exists between that station and the next station upstream. The order of stations is G H I B 1 2 3 4 C 5 6 A 7 8 9 E D so a beacon from station 5 would indicate a problem with station C. A Secondary station that is offline or even powered down will not cause a beacon message because the Link repeater will bypass the station and maintain link continuity.

Inside the door covering the Multibus chassis, interrupt and task activity can be observed in the LEDs of the annunciator panel. If no activity is seen, the Primary is down. This is unusual because both the software and the hardware try to restart the system under normal failure modes. Note that these systems will not be found in mode where the processor is randomly executing meaningless data; the 68000 will typically enter its halt state if it receives two bus errors or address errors in a row. If the system tries to restart itself after an error condition and finds that it has had fifteen such conditions within the past hour, it will halt. A manual reset will allow the processor to start, but how long it runs will depend upon when it receives its fifteenth abort within a one hour period. Typical error or abort conditions include bus errors, address errors, unimplemented interrupts, illegal instructions and trap errors.

If the primary is found to be halted, the operator may try to RESET it, but if it does not start a more severe problem exists and someone should be called. There may be some helpful clues on the Primary console or on the Link Driver TV display.

6.3 SUPERFICIAL VIEW OF A SECONDARY

A Secondary station contains a single 68000 processor. As with the Primary, the interrupt and task level activity can be observed from the front of the Multibus chassis. No activity indicates the processor is halted and only a reset will restart the processor.

When a Secondary is operating, activity will be seen on the LEDs of the communicator panel, and the S-H/A-D chassis below the Multibus bin. The LEDs will exhibit a 15 Hz repetitive pattern that is nearly identical in all stations. The green LED on the front of the local console should also flash at 15 Hz.

A Secondary that is suspected of malfunctioning may be reset to see if the problem disappears. Some of the LSI chips in the system are software configurable and on rare occasions the internal configuration may be changed by some severe external perturbance - like a lightning strike.

When checking on a Secondary, the status of its Link Repeater chassis should also be checked to insure that the station has not been bypassed. A bypass condition is indicated by the large red "BYPASS" LED on the Link Repeater front panel, and the cause of the Bypass condition is shown by small yellow LEDs. The secondary's yellow "TX CLK ENABLE" LED should be off. (Only the Primary TX CLK ENABLE LED will be on for normal operations). Constant or 15 Hz activity should be observed on the green indicators of the Link Repeater chassis. A Secondary's TX CLK ENABLE indicates the local station is sending a Beacon message because it is not receiving data from upstream.

If local parameters are available on the local console, but no remote data is displayed, the problem is related to communications. If some, but not all, remote data is available, the problem is with the stations that do not respond - the link and local station are probably OK.

6.4 WHAT DOES A RESET DO?

A reset will restart the 68000 from the very beginning of the program. There is no attempt to perform a "warm" Reset - all resets, whether generated by software or hardware, manual or automatic, perform the same restart of the system. During initialization all the analog and digital settings are sent to the hardware, but in general no effect will be observed in the external equipment because the settings are the same as those stored in the hardware. When a Secondary is powered up it retransmits the analog and digital settings from non-volatile RAM where they are stored.

A Reset will also reinitialize all the programmable LSI controllers in the system. In general, if a system is suspected of malfunctioning it may be reset to see if the apparent problem disappears.

6.5 A VIEW FROM THE ALARMS SCREEN

Alarms and Limit monitoring of Linac analog and digital parameters has been operational since the system was installed. Each Secondary provides the monitoring function for its own parameters and the necessary alarm messages are collected by the Primary stations. Each channel can be monitored to inhibit Linac beam for out-of-tolerance parameters. Because each station has only its own parameters to monitor, only a few milliseconds (4 ms typically) are spent to perform this task. All channels are monitored every Linac cycle and beam is inhibited on the next cycle if necessary.

6.5.1 The Alarm Messages

The format of analog and binary alarm messages that appear on the alarm screen contains the date and time, cycle number, and name or descriptor.

Usually the alarm messages relate to Linac devices, but self checking features of the system cause alarm messages that indicate problems with the systems themselves. Of particular interest are the "SEC #n OFFLINE" and the "SEC #n RESET".

6.5.1.1 The OFFLINE Message -

The SECONDARY #n OFFLINE message is generated by the Primary whenever a Secondary fails to respond to a test poll. One of the possible 32 Secondaries is sent a test poll each fifteenth of a second, so every station will be tested every two seconds. A binary status bit is set or cleared by the Primary to record the response received from each station. These status bits are then monitored with the 2x filter to inhibit beam for improper response received from the existing stations.

A Secondary can be "OFFLINE" for many reasons; powered down, halted, manually bypassed, automatically bypassed, being reset, faulty communication board, and SDLC link problems can all cause OFFLINE messages. In general, it's a bad omen and bears watching.

6.5.1.2 The RESET Message -

The SEC #n RESET message is a comment that is generated by the Secondary to announce that it has just been Reset and reported by the Primary along with Analog and Binary alarms. During the reset of a Secondary, that Secondary may not receive a test poll and therefore an OFFLINE condition may not be detected. However, a Secondary that has been reset, for whatever reason, will voluntarily send the RESET message. These messages are rare and indicate some traumatic experience at the Secondary. They have been observed occasionally during heavy crowbar activity of an RF system or severe arcing of the Preaccelerator. The RESET comment may, but need not, be accompanied by an OFFLINE message. The time associated with the RESET message is the time last known to the system before it RESET; hence it is the time the system wenr down. At each even minute, the time of all systems is updated with the value received from the NBS clock in the Main Control Room.

6.6 THE TDATA CONNECTION

Most Linac Parameters are sampled and held at a variable time, TDATA, that normally occurs at 2000 us into the cycle. It is generated by a variable timing channel in system B, buffered by a pulse repeater, driven down the entire length of the Linac, and transformer coupled at each station to trigger the sample and hold amplifiers. When TDATA fails for two successive Linac cycles, several hundred messages will be generated and the alarms screen will begin to scroll indicating all manner of bad news. Such a flood of messages usually suggests a problem with TDATA. One simple check can be made to determine if the variable timer has failed. At relay rack LE1-RR2-10 a panel has been installed to allow the TDATA pulse repeater to get its input from the variable TDATA or from a manual predet pulse called T2000. As its name suggests, T2000 arrives at 2000 us and the use of this pulse could allow continued operation of the Linac if the variable TDATA fails. Selecting between the two sources is done by simply moving a BNC cable from TDATA to T2000.

6.7 ETHERNET

The Linac Primary to PDP-11 Front End Host connection is made using an Ethernet link. Besides being a fast, widely accepted international standard for intercomputer communication, Ethernet has the prominent feature of being supported by commercial suppliers who make interface cards for both Unibus and Multibus. Ethernet is a half duplex, serial, 10 megabit protocol. By way of the Ethernet

interface, requests for data from Host computers are sent to the Linac Primary and answers are collected and returned to the host by the primary at the specified repetition rate. For repetitive data, the host only needs to ask once and data will be returned till the request is cancelled. A typical parameter page on a console will cause a short (~200 us) burst of data to be returned at 15 Hz.

Because an Ethernet cable can support many (up to 100) nodes, multiple Host Computers can be connected simultaneously. The Hosts "learn" the (6 byte) address of the Primary from a broadcast transmission that is sent by the Primary at 17 sec intervals. The Primary remembers the address of the Host that was included in the request for data so the answers may be returned to the proper address.

In the Linac system there are only two Hosts - the Front End PDP-11 and a 68000-based Host located next to Sec 3 in relay rack LE3-RR3-1.

The Ethernet connection has been very trouble-free particularly since the new generation controller card was installed in the PDP-11. However, if trouble with the Ethernet link is suspected, a quick check of the 68000-based Host can determine whether the Link is working or not. This Host operates in the same way as a normal secondary, except that its only connection with the system is to the Primary via the Ethernet cable. If the 68000 Host can get data from the Primary, the Ethernet link works. In that case, the suspected problem must be related to the Front End.

6.8 REPLACEABLE PARTS AND SPARES

Considerable effort has gone into making the Linac system very modular and easy to service. The Link Repeaters, S-H/A-D converters and D-A converters are housed in external chassis.

6.8.1 Linac Spares

Hot spares for the Linac system are available in System A, the Linac test station. This system is normally powered on with a full complement of cards and chassis. Binary I/O cards, CPU and communication cards from this system should operate in any station. Spare ADs and DAs are also maintained in this area. Note that the contents of the core memory cards are peculiar to each station because this memory contains the data base. Although System A is a source for a "known good" core memory, the contents would have to be downloaded from the VAX if the core memory is moved to another station.

Another viable, but less certain source of warm spares is the small Primary-and-2-Secondaries test setup in the lab at Linac station 2. This setup is maintained to test cards offline. It is also a source for spares for the Primary station.

A third source for spares is in a cabinet near 7835 for Linac system 2. An attempt is being made to outfit this cabinet with spares that have seen several months of continuous service online in the system.

6.8.2 Changing A-D And D-A Chassis

If an A-D or D-A chassis has been determined to be faulty it may be replaced with a spare. Two Burndy 8-conductor coax connectors, a ribbon cable, one BNC cable and the AC cord are unplugged and the chassis is free to be swapped with the spare. The chassis address switch setting of the spare should be set to match the unit being replaced. Two types of A-D chassis exist, +2.5V F.S. and +10V F.S. The 2.5V units are identified by an obvious red label in the upper right corner of the front panel. Only one of the 2.5V units is used per system and they are used only in systems 1, 2, 3, 4, 5, 6, 7, 8, 9, B and D.

D-A chassis are nearly identical to replace. They also have a chassis address switch that must match the online unit being replaced.

6.8.3 Local Console Replacement

Local consoles are connected to the system by three BNC coax cables; transmit, receive and composite video. All consoles are identical so any malfunctioning console may be replaced with a spare. Since the architecture of the Linac system allows any parameter to be accessed from any terminal, the consoles at neighboring stations can be used, in many cases, to accomplish local control.

6.8.4 Replacing Multibus Cards

Only normal care must be exercised to replace Linac system Multibus cards. Because Multibus uses printed circuit edge connectors, the bin must be powered down before replacing cards. Some cards access a reset line on the upper, P2, connector, so care should be exercised to locate the replacement card in the same slot as the original.

Two types of binary I/O cards exist although they differ only in the arrangement of input and output bytes. The two types are identified by red or blue dots on the card ejectors. When replacing binary boards, the original must be replaced with the same type.

6.8.5 Primary Station Precautions

The Linac Primary is a dual processor system and contains the Link Driver and the Primary Console CPU cards in slots 12 and 11 respectively. They each have communication cards in slots 10 and 9. The Link Driver connects to a fiber optic link repeater chassis but has no console; the Primary Console CPU has a local console connection but does not attach to a link repeater.

When replacing CPU and communication cards in the Primary station, spares should be taken only from the test station Primary in the lab. Interrupts and software for the Primary differ from a normal secondary. The Primary in an SDLC system operates in full duplex rather than the loop mode used in Secondaries, so the Fiber Optic Link Repeater chassis is special for the Primary. Because all messages originate in the Primary, the link repeater chassis is the source of the 1 MHz clock used for the entire link. Its "TX CLK ENABLE" LED is always on (the secondary TX CLK ENABLE LEDs are off unless the station is transmitting a beacon message).

The primary contains one binary I/O card it uses to inhibit beam. This is a standard (red dot) binary I/O card.

6.8.6 Alarm Terminal

For reporting alarms, the primary console outputs the messages using ACIA-2, an RS232 port on the Primary console CPU. These messages go to a TEK terminal and the video is buffered to the Main Control Room. In case of failure, a second TEK terminal is available. Both are located in the relay rack with the Primary station (LE6-RR2-1).

6.8.7 Ethernet Controller

The connection to the Linac Front End PDP-11 is made using Ethernet. The Ethernet controller board is located in slot 2 of the Primary Multibus bin and connection to the transceiver cable is by way of a 16 conductor ribbon cable. The 68000-based Host in Area 3 has an identical controller that is available for use as a hot spare.

Another viable, but less certain source of warm spares is the small Primary-and-2-Secondaries test setup in the lab at Linac station 2. This setup is maintained to test cards offline. It is also a source for spares for the Primary station.

A third source for spares is in a cabinet near 7835 for Linac system 2. An attempt is being made to outfit this cabinet with spares that have seen several months of continuous service online in the system.

6.8.2 Changing A-D And D-A Chassis

If an A-D or D-A chassis has been determined to be faulty it may be replaced with a spare. Two Burndy 8-conductor coax connectors, a ribbon cable, one BNC cable and the AC cord are unplugged and the chassis is free to be swapped with the spare. The chassis address switch setting of the spare should be set to match the unit being replaced. Two types of A-D chassis exist, +2.5V F.S. and +10V F.S. The 2.5V units are identified by an obvious red label in the upper right corner of the front panel. Only one of the 2.5V units is used per system and they are used only in systems 1, 2, 3, 4, 5, 6, 7, 8, 9, B and D.

D-A chassis are nearly identical to replace. They also have a chassis address switch that must match the online unit being replaced.

6.8.3 Local Console Replacement

Local consoles are connected to the system by three BNC coax cables; transmit, receive and composite video. All consoles are identical so any malfunctioning console may be replaced with a spare. Since the architecture of the Linac system allows any parameter to be accessed from any terminal, the consoles at neighboring stations can be used, in many cases, to accomplish local control.

6.8.4 Replacing Multibus Cards

Only normal care must be exercised to replace Linac system Multibus cards. Because Multibus uses printed circuit edge connectors, the bin must be powered down before replacing cards. Some cards access a reset line on the upper, P2, connector, so care should be exercised to locate the replacement card in the same slot as the original.

6.9 ANOMALIES AND LITTLE KNOWN FACTS

As with any system, there are a few curiosities in the operation of some of the equipment.

6.9.1 MADC Module

On rare occasion, an MADC module used in the A-D chassis reports a full scale value for all of its sixteen analog channels. Although Analogic denies that such a thing can happen, we have observed the effect a few times. It happens only when the chassis is being powered up and the cure is to power cycle the chassis. In normal operation the A-Ds are never turned off so the effect will only happen when recovering from a power outage.

6.9.2 Ethernet Controller

In the past, the Multibus Ethernet controller has been observed in a state where it fails to transmit. Status of the board (address V:1E001) indicates the transmit buffer is being used to transmit. The proper status is $CC; the anomalous value is $EC. This fault is cleared by unplugging and replugging the 16-conductor ribbon cable on the card edge. Again, the manufacturer claims never to have seen this effect. Power cycling the primary will also clear the fault, but a reset of the primary does not effect it.

CHAPTER 7

SYSTEM DETAILS

This section contains details of the implementation and is included here for completeness.

7.1 THE MULTIBUS BIN

The Multibus chassis used in all Linac stations is a standard Intel ICS-80. The 4-wide card cages are not used, but have been replaced by an Electronics Solutions 12-slot card cage and backplane. This was done to eleminate the segmented backplane that comes from stacking three of the 4-slot backplanes; Electronic Solutions 12-slot backplanes are continuous. Also, a 12-slot backplane in an ICS-80 chassis gives a board spacing of 0.75 inches, instead of the normal 0.6 inches, to allow better cooling. The ICS-80 chassis itself was chosen because of the vertical format and front access to the Multibus cards. Vertical card orientation improves cooling air flow and reduces board warpage.

The ICS-80 chassis has a key-operated power switch and two push buttons labeled "RESET" and "INTR". The signal generated by the INTR pushbutton connects to the INT7 (Pin P1-36) of the Multibus backplane. It causes a Level 7 interrupt on the CPU board, which is the highest priority, non-maskable interrupt. The Level 7 Interrupt service routine causes a restart of the program.

The RESET pushbutton connects to pin 38 of the P2 connector -- a pin designated as external RESET by Intel. (This pin has since been reserved by the IEEE-796 committee, and subsequently redefined by Intel as part of the iLBX bus.) In the Linac system, pin 38 of P2 connects to the slots occupied by CPU cards, timer boards and core memory boards. Both the core memory and the timer boards are capable of initiating a system reset.

7.2 LOCATION OF SECONDARY STATIONS

Secondary stations are located close to the equipment they control, usually in the same bay of relay racks with the end rack containing the AMP terminal strip. The location of each secondary is listed below.

Sec. #	Location
1	LE1-RR4-2
2	LE2-RR4-2
3	LE3-RR3-2
4	LE4-RR3-2
5	LE5-RR3-2
6	LE6-RR3-2
7	LE7-RR2-2
8	LE8-RR2-2
9	LE9-RR2-2
A	System 10 Area
B	LE1-RR2-9
C	LU5 Area
D	Booster Gallery
E	LQ1 Area
G	H- Control Racks
H	H- HV Dome
I	I- HV Dome
Pri.	LE6-RR3-1
Host	LE3-RR3-1

Note that the Secondary numbers are mnemonically chosen and are different from the installed order on the loop. The order of Secondaries around the loop is:

G H I B 1 2 3 4 C 5 6 A 7 8 9 E D

This order on the loop is necessary to identify the location of a problem when a "Beacon" message is received by the Primary.

7.3 PRIMARY/SECONDARY INTERRUPT LEVELS

Interrupt levels for the Primary Console, Link Driver, and Secondary Stations are listed IN Table 7.3. The INTn values are the Multibus backplane interrupt lines. Unless otherwise noted, the INTn line used is the same as the interrupt level. Unused interrupt levels are connected to the INT0 line on the backplane. The timer interrupt lines are from the MC6840 that is on the CPU board. PIA chips are also on the CPU card, but these interrupt levels are input using the Lemo connectorson the display panel. The front panel board includes circuitry to condition external strobes before inputting to the control line inputs of the PIA.

LEVEL	SECONDARY	PRI. CONSOLE	LINK DRIVER
7	ICS-80 INT	ICS-80 INT	ICS-80 INT
6	ADLC/DMA		LINK RECEIVE
5			
4	SER. CONSOLE	SER, CONSOLE	SER. CONSOLE (INT3 Line)
3		ETHERNET (INT2 LINE)	
2	CONSOLE/MOTOR	CONSOLE/MOTOR	CYCLE EVENT
1	15 HZ	15 HZ	15 HZ

TABLE 7.3 Interrupt Assignments for Linac Stystems

7.4 BEAM INHIBIT/ BEAM ENABLED

Some Linac parameters are monitored to turn off the beam if out-of-tolerance conditions are found. The mechanism for inhibiting beam should not depend upon the link or any other Secondary, so a hardwired "open collector" type connection is made between the pulse shifter electronics and the Secondary stations. A three pair cable is daisy-chain connected to each Secondary. One pair is dedicated to beam inhibit; one for informing each Secondary that the beam is enabled; one is spare.

The Inhibit signal is powered in the Preaccelerator area and connected to an output OPTO22 at each Secondary. Any Secondary can then short the pair, resulting in an inhibit signal for the pulse shifter.

The Beam Enabled signal is powered in the Preaccelerator area and detected by an OPTO22 input module at each Secondary. The beam enabled signal is used by the Secondary to differentiate between beam and no-beam cycles.

7.5 MEMORY MAPS FOR CPU BOARD

The memory map shown in Figure 7.5 is the map used for all Secondary stations and for the Primary console. The organization of memory is determined by the programmable logic devices on the CPU card. Eight memory socket pairs on the CPU card are mapped for 2 Kbyte RAM chips in socket pairs 0,1,2, and 3 and for 8 Kbyte PROMS in socket pairs 1,2,...,and 7. Secondaries now have 8 Kbytes of scratch RAM in pairs 0 and 1, leaving space for 96 Kbytes of PROM space (64 Kbytes are currently installed). The 32 Kbyte core memory board at $10000 is the only offboard RAM used in Secondary stations. The Primary system has a 128 Kbyte RAM board located at $40000.

With reference to Figure 7.5, the video RAM block at $4000 is an offboard memory area. The video RAM and peripheral registers on the communication board occupy $400 memory locations. All systems have communication card at $4000 and the Primary has a second communication card at $4400 for use by the Primary Link Driver.

Onboard I/O is at $5000. Because a 68000 has no I/O instructions, a separate block of memory is decoded and assigned for use as Multibus I/O. This block, from $6000 to $6FFF, transfers data using the Multibus IORC and IOWC strobes on the backplane. To the 68000, I/O is just a block of memory.

7.6 BINARY I/O BOARD CONFIGURATION

All binary I/O is supplied by two nine-byte boards that are the same except for the arrangement of buffers and resistor terminations on the interface lines. Figure 7.6 shows the configuration of buffers, latches and resistors for the two board types. The Buncher system (B) has an additional (blue dot) board installed to operate the stepping motors associated with the emittance probes.

7.7 PIA ASSIGNMENTS

The parallel I/O facilities of the 68000 CPU board are used for the front panel. Two PIAs provide four bytes of binary I/O and eight control lines. The A side of each PIA is used for binary input to sense an eight pole DIP switch. The B sides are configured for outputs, buffered, and used to drive LED indicators and test points that show the interrupt and task activity of the 68000. Only four of the eight control lines are used. Interrupt signals can be input on Lemo connectors on the front panel. These drive the CA1 inputs of the two PIAs. The CA2 outputs are

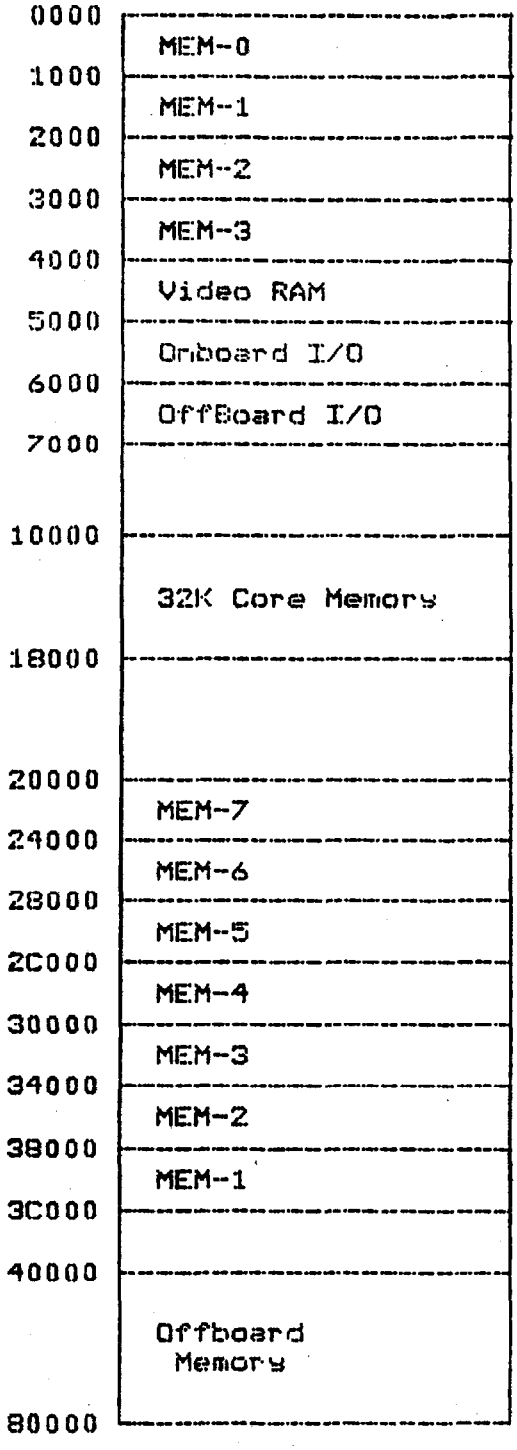


FIGURE 7.5 Memory Map for Linac CPU Boards

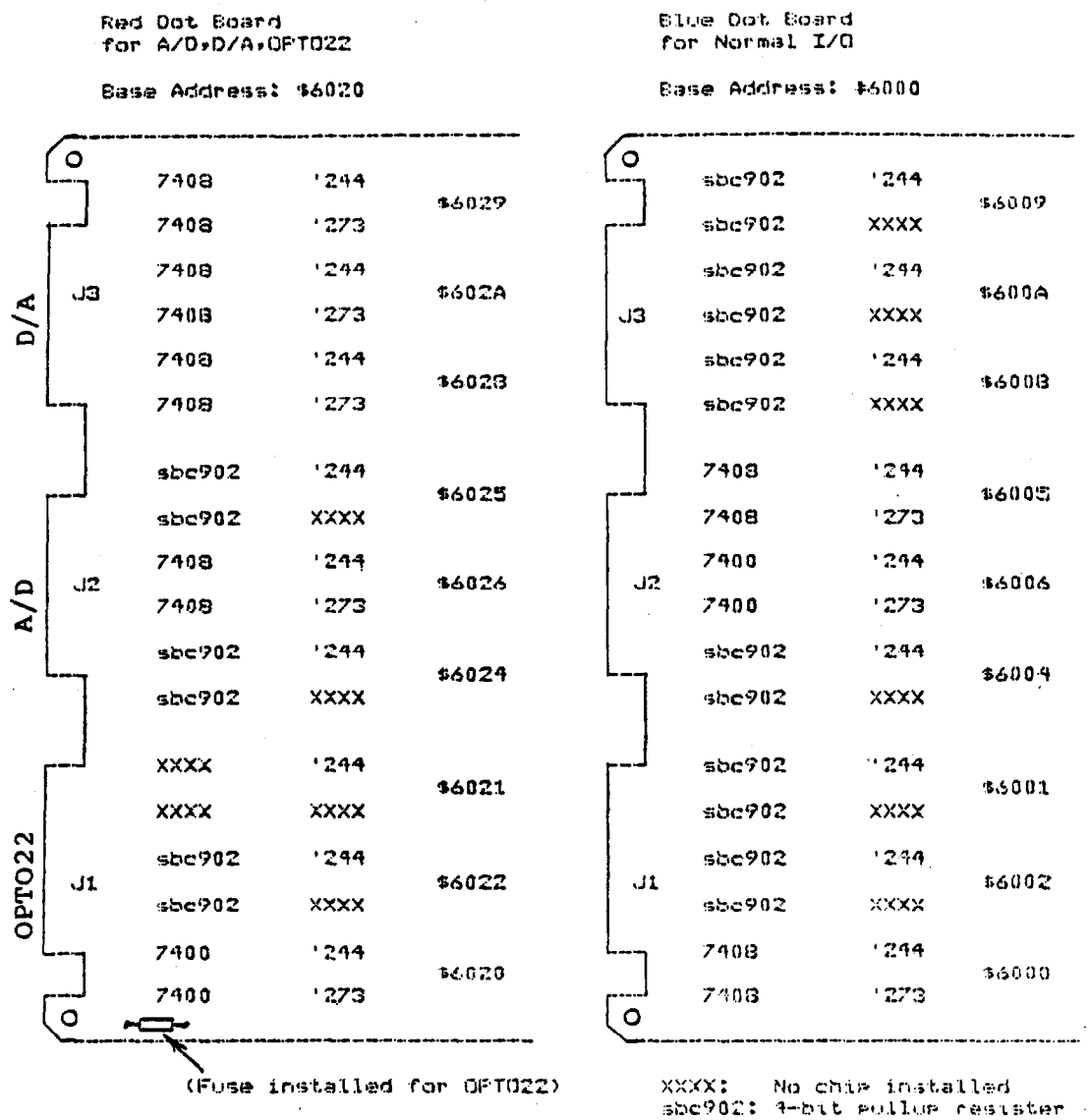


Figure 7.6 Buffer Arrangement for Binary I/O Cards

DATE: 8/03/83

PIA 1 A-SIDE: 68000 SYSTEM STATION ADDRESS

ADDRESS: DATA REGISTER 5041 ; CONTROL REGISTER 5045
CONFIGURATION: DATA DIR REG. 00, CONTROL REG. 04

CONTROL BITS: CA1- NOT USED
CA2- NOT USED

DATA: PA 7- SPARE
PA 6- SPARE
PA 5- SPARE
PA 4- STATION ADDRESS BIT 4
PA 3- STATION ADDRESS BIT 3
PA 2- STATION ADDRESS BIT 2
PA 1- STATION ADDRESS BIT 1
PA 0- STATION ADDRESS BIT 0

PIA 1 B-SIDE: 68000 SYSTEM INTERRUPT LEVEL INDICATORS

ADDRESS: DATA REGISTER 5043 ; CONTROL REGISTER 5047
CONFIGURATION: DATA DIR REG. FF, CONTROL REG. 04

CONTROL BITS: CB1- NOT USED
CB2- NOT USED

DATA: PB 7- SPARE
PB 6- 6854/6844 SDLC/DMA INTERRUPT ACTIVITY
PB 5- SPARE
PB 4- 6850 SERIAL CONSOLE RECEIVE
PB 3- SPARE
PB 2- 6840 TIMER (MOTOR INT, CONSOLE INT)
PB 1- 6821 PIA-0 15 HZ INTERRUPT
PB 0-

TABLE 7.7a Bit Assignments for PIA1

DATE: 8/03/83

PIA 2 A-SIDE: 68000 SYSTEM MODE SWITCHES

ADDRESS: DATA REGISTER 5040 ; CONTROL REGISTER 5044
CONFIGURATION: DATA DIR REG. 00, CONTROL REG. 07

CONTROL BITS: CA1- 15 HZ INTERRUPT
CA2- NOT USED

DATA: PA 7- SBUG/SYSTEM SELECT ON RESET
PA 6- INHIBIT AUTO SETTING RESTORE
PA 5-
PA 4-
PA 3- MESSAGES TO ACIA2
PA 2- MESSAGES TO CONSOLE
PA 1- ALARMS INHIBIT
PA 0- COMPUTER SDLC LINK BYPASS

PIA 2 B-SIDE: 68000 SYSTEM TASK INDICATORS

ADDRESS: DATA REGISTER 5042 ; CONTROL REGISTER 5046
CONFIGURATION: DATA DIR REG. FF ; CONTROL REG. 04

CONTROL BITS: CB1- NOT USED
CB2- NOT USED

DATA: PB 7- MESSAGE MONITOR
PB 6- DATA LIST UPDATING
PB 5- DATE AND TIME
PB 4- SMALL MEMORY DUMP
PB 3- APPLICATION PROGRAM
PB 2- CONSOLE PROCESSING AND KEYBOARD INTERRUPT
PB 1- ALARMS AND CLOSED-LOOPS
PB 0- PROCESS LINK COMMANDS

TABLE 7.7b Bit Assignments for PIA2

DATE: 8/03/83

OUTPUT BYTE ADDRESS: $6020

OPTO22 TERMINAL # SIGNAL,RTN	BINARY I/O CONNECTOR PIN #	BIT #	FUNCTION
1,2	47	0	BEAM INHIBIT
3,4	45	1	COMPUTER ENABLE
5,6	43	2	
7,8	41	3	
9,10	39	4	QUAD RESET
11,12	37	5	SYSTEM RESET
13,14	35	6	HV OFF
15,16	33	7	HV ON

INPUT BYTE ADDRESS: $6022

OPTO22 TERMINAL # SIGNAL,RTN	BINARY I/O CONNECTOR PIN #	BIT #	FUNCTION
17,18	31	7	BEAM ENABLED
19,20	29	6	SPARE DAISY CHAIN INPUT
21,22	27	5	SPARE
23,24	25	4	SPARE
25,26	23	0	SPARE
27,28	21	1	SPARE
29,30	19	2	SPARE
31,32	17	3	SPARE

NOTES: 1. ALL EVEN CONNECTOR PINS ARE COMMON
2. CONNECTOR PIN #49 IS FUSED +5 VOLTS
3. ALL DC INPUT SIGNALS ARE ASSUMED POSITIVE

TABLE 7.8 Bit Assignments for OPTO22 I/O

buffered to Lemo connectors on the front panel. The CB1 and CB2 signals are not used. PIA configuration data and bit assignments are given in Table 7.7.

7.8 OPTO22 ASSIGNMENTS

A 16-channel OPTO22 mounting rack is installed in each Secondary. Eight bits of input and eight bits of output are available. For completeness, the pin assignments and OPTO22 terminal numbers are documentedin Table 7.8 below along with the current bit assignments for a typical station that includes an RF system.

7.9 MISCELLANEOUS ADDRESS ASSIGNMENT

This section lists the addresses that have been assigned to various devices in the Linac system. They are included here for reference.

7.9.1 Communication Board Addresses

The base address of the Communication card is $4000. Listed in Table 7.9.1 are the base addresses of the LSI chips along with the address of various registers on the board. Bit assignments for the registers are included. Registers internal to the LSI chips are addressed as described in the Motorola data sheets with the base address added as an offset.

Addr.		Function
$4000	R/W	Video RAM
$4200	R/W	Tx,Rx FIFO
$4220	R	Misc. Status
$4240	R/W	Parallel Tx,Rx FIFO
$4260	R	FIFO Status
$4260	W	FIFO Clear
$4300	R/W	ACIA Base Address
$4340	R/W	DMA Base Address
$4380	R/W	SDLC Base Address

TABLE 7.9.1a Communication Board Addresses

Bit No.	Function
7	
6	
5	
4	
3	Clear SDLC Rx FIFO
2	Clear SDLC Tx FIFO
1	Clear Parallel Rx FIFO
0	Clear Parallel Tx FIFO

FIFO Clear Register ($4260 Write)

Bit No.	Function
7	IR SDLC Rx FIFO
6	OR SDLC Rx FIFO
5	OR SDLC Tx FIFO
4	IR SDLC Tx FIFO
3	IR Parallel Rx FIFO
2	OR Parallel Rx FIFO
1	OR Parallel Tx FIFO
0	IR Parallel Tx FIFO

IR=Input Ready
OR=Output Ready

FIFO Status Register ($4260 Read)

Bit No.	Function
7	TV Ready
6	FLAG DETECT Missing
5	Link Bypass
4	
3	
2	
1	
0	

Miscellaneous Status Register ($4220 Read)

TABLE 7.9.1b Bit Assignments for Comm. Controller Registers

7.9.2 Timer Board Addresses

The timer board contains three Motorola 3-channel timer circuits and the system watchdog timer. A WRITE operation to the watchdog timer address triggers a one-shot; the data is ignored. Addresses for this board are listed below.

Addr.	Function
$6100	TIMER CHIP 0 BASE ADDRESS (CHAN 0,1,2)
$6108	Timer Chip 1 Base Address (Chan 3,4,5)
$6110	Timer Chip 2 Base Address (Chan 6,7,8)
$6118	Watchdog Timer Trigger

APPENDIX A

THE MC68000-BASED SINGLE BOARD COMPUTER

The MC68000 CPU board used in the Linac Control System is described in Fermilab FN-330.

APPENDIX B

THE LINAC COMMUNICATION CONTROLLER

B.1 GENERAL INFORMATION

A multifunction Multibus compatible communications controller has been developed for use in the Linac control system. Figure B.1 is a block diagram of this controller. Included on the board are:

Synchronous Data Link Controller (SDLC)
Direct Memory Access controller (DMA)
Byte Serial I/O port
Asynchronous serial port
Video RAM display generator

In operation the Communication controller connects the local Linac stations to the SDLC link repeater chassis, and supports the local console.

B.2 DESIGN CONSIDERATIONS

B.2.1 The Bus Interface

The controller board is designed to be compatible with the Multibus/IEEE-P796 with Compliance characteristics Master D8 M20 and Slave D8 M20 V0. That is, it operates either as a Slave or Master (when performing DMA), decodes/drives 20 address lines, uses only an 8-bit data path and is the source of non-vectored interrupts. Because an 8-bit data path is used, the board can be operated by either 8 or 16-bit processors. The schematic diagram is given in Figure B.2.1.

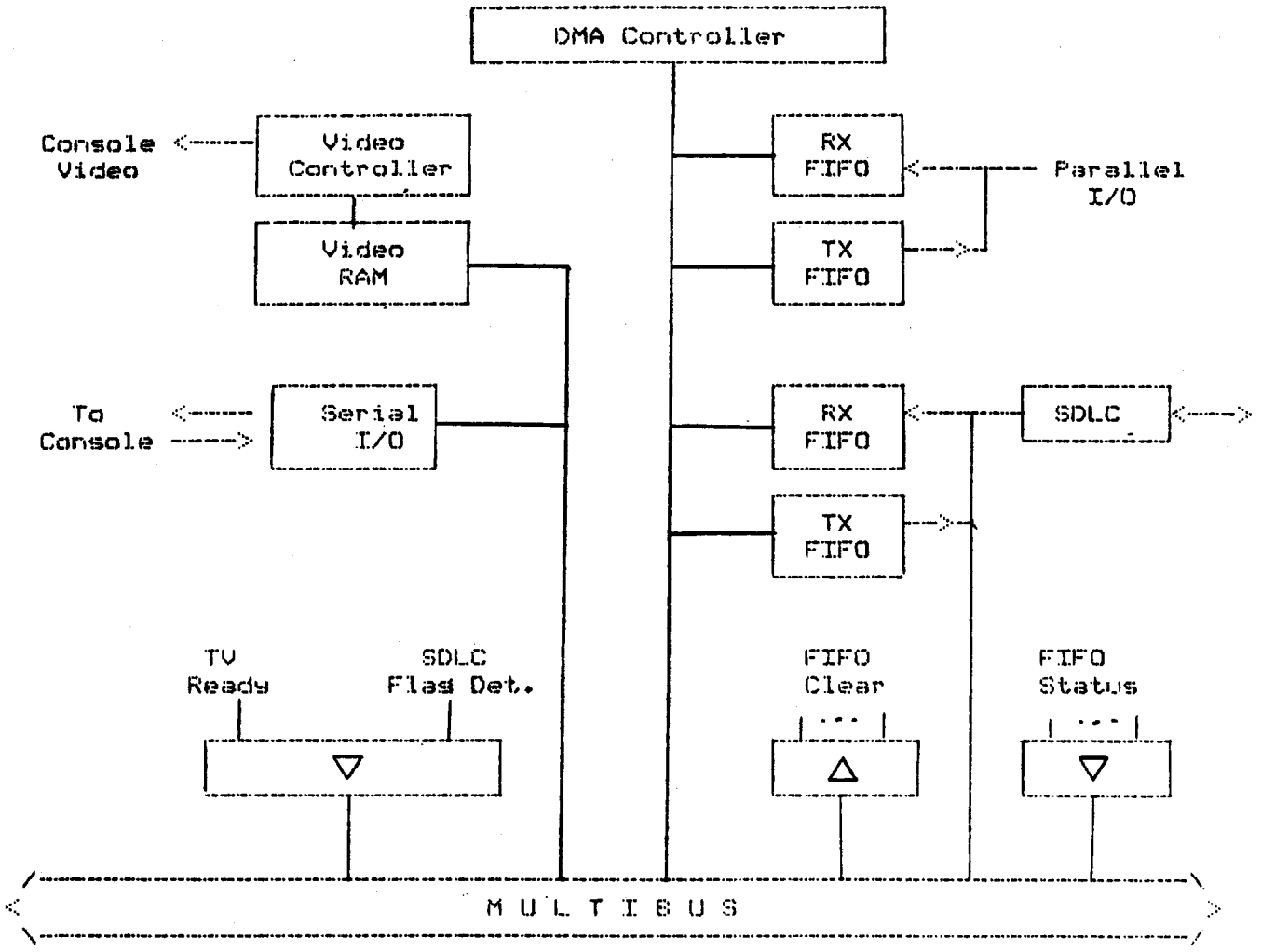


Figure B.1 Block Diagram of Communication Controller

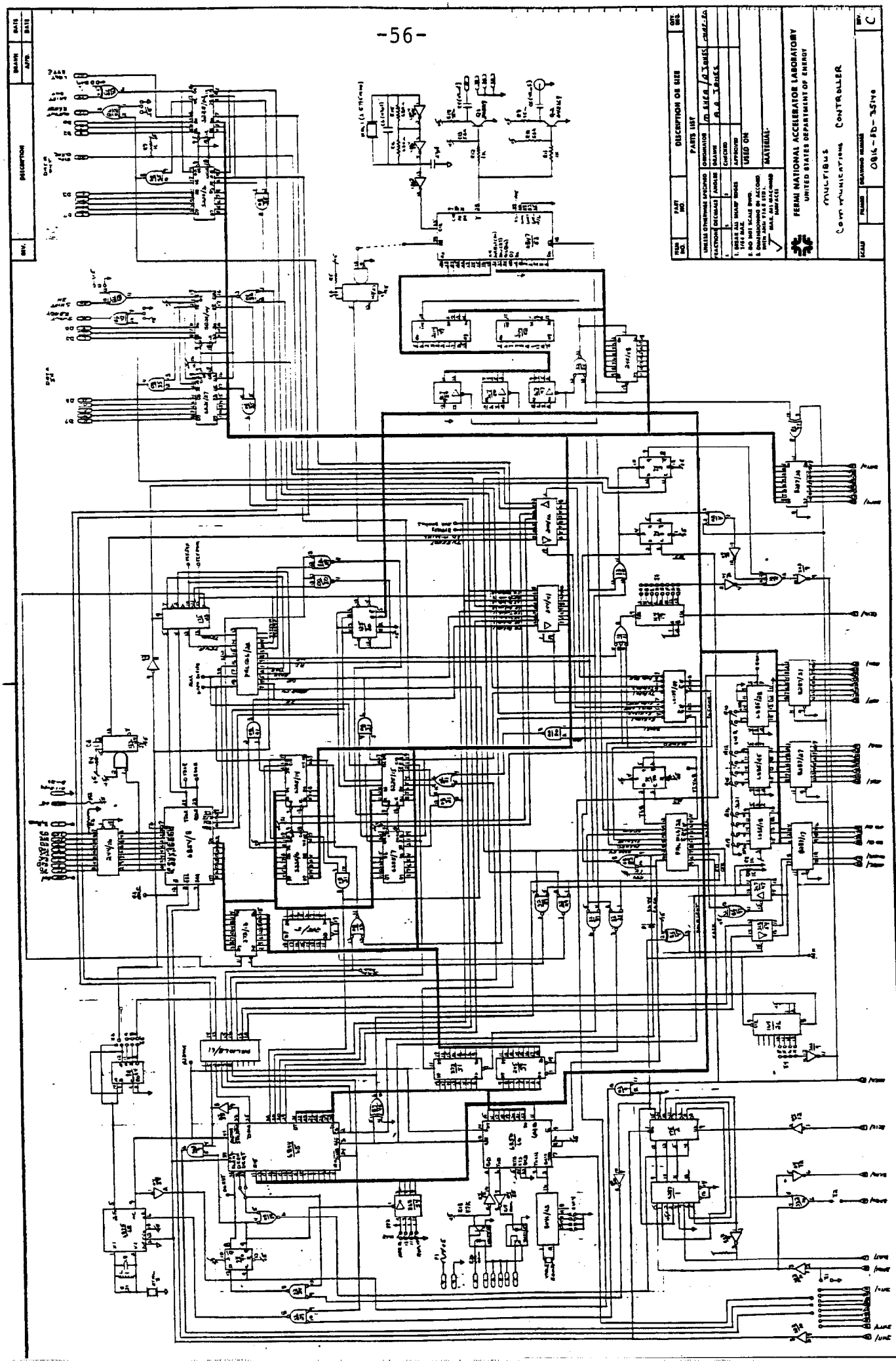


Figure B.2.1 Circuit Diagram of Communication Board

B.2.2 Console Support

The Communicationn board includes circuity to support the local consoles of the Linac Secondary stations. The console provides an alphanumeric video display, keyboard, shaft encoder knob and a selection of lighted pushbuttons. Appendix D describes this console.

B.2.3 Video Generator

The video generator is built around an LSI video display driver, the MC6847. Although designed for video games, the circuit has a 16 line by 32 character alphanumeric mode that is used for this application. All of its features are preprogrammed and the character generator, shift register, and address counters are all internal so that only a clock (3.5795 MHz) and 512 bytes of display RAM are needed for the chip to output the composite video signal. For simplicity, the processor accesses the display RAM during horizontal retrace time to avoid flicker on the screen.

B.2.4 Console Serial I/O

A Motorola MC6850 ACIA is used for the serial connection to the console. Because the console operates at a slow (4800) baud rate the 6850 is allowed to interrupt the processor to signal that data from the console is available. Opto-insolators are used in the transmit and receive lines to decouple this board from the remote console. Current for these are driven from the console chassis.

B.2.5 SDLC/DMA

Data received and transmitted on the 1 MHz link are transferred to and from memory under DMA control. This data rate corresponds to one byte per 8 us for one channel (Tx or Rx). Operation of the Primary station requires simultaneous operation of the transmit and receive channels, giving a data rate of 4 us per byte. To allow this data rate without placing severe restrictions on all Multibus cycle times, some on-board buffering was needed. A 16 byte FIFO is provided in each DMA channel and transfers by the DMA controller are made between these FIFO buffers and offboard memory. The DMA gains access to the bus by normal multi-master bus arbitration logic on the board. In this way the synchronous SDLC chip transfers of data to the FIFOs are decoupled from the bus cycles and thehe 1 MHz data rate can be supported without providing large RAM buffer space on

Outputs CSENRD and CSENWR are chip selects for a 74139 that selects the asynchronous registers on the board; TX and RX FIFO's, status registers and the FIFO clear register.

Multibus accesses to the 6854 are indicated by the ADDR54 output, but these accesses must be arbitrated with the autonomous transfers between the 6854 and the TX,RX FIFO's. A 12L6 PAL shown in Fig. 4. performs this arbitration.

B.3.3 I/O Connectors

These card edge I/O connectors are used for the serial port, the parallel port and the console I/O. Also a Lemo coaxial connector is available to drive a second TV monitor with the information displayed on the console.

Connector J1 carries the I/O for the SDLC link. In addition to the TX and RX clock and data lines, this connector carries the Flag Detect signal and Secondary power and ground to the link repeater chhassis. of J1 is given in Table 1.

J2 is the interface to the byte serial section of the board.

J3 connects the console serial Transmit and receive, and the composite video signal to the console chassis.

B.3.4 Miscellaneous Registers

Three miscellaneous registers are availabble on the board. The bit definitions of these registers are given in Table 7.9.1. Writing a "1" to a bit in the FIFO clear register clears the associated FIFO. The value of the bit locations of the FIFO status register reflects the state of the individual input ready and output ready signals of the FIFOs. A "1" means ready.

In the miscellaneous status register, the MSB is a signal derived from the horizontal sync output of the 6847. This bit allows the software to store data in the Video RAM only during the horizontal retrace time.

Bit 6 of Misc. Status is driven by a 100 ms one-shot that is retriggered by flag detect pulses from the 6854. A "0" indicates no flags were detected for 100 ms.

Link Bypass is an input from the Link Repeater chassis that allows the processor to determine if the station is being bypassed. A "0" means bypassed.

B.4 DMA OPERATION

The 6844 DMA controller is operated in the four channel mode, transferring data between the various FIFOs and memory. during the DMA memory accesses, the upper address lines are asserted to reflect the setting of the 4-bit dip switch S3. This is necessary because the 6844 drives only 16 address lines. Because the upper four address lines are set by switches, all DMA transfers are constrained to lie within a single 64K block of address space.

For DMA cycles, shift-in/shift-out pulses for the selected FIFO are generated by IC61, a PAL10L8. Normal Multibus access is provided so the FIFOs can be written and read by the processor.

An SDLC controller chip must be told when the last byte of a message is transferred to it, so the 16 bit frame check sequence and terminating flag can be appended to the bit stream. In the 6854 this is accomplished by storing the last byte in the Frame Terminate registrer rather than the Frame Continue register used for all other bytes of the message. The last byte flag is stored in the FIFO by the DMA controller. This flag then progresses through the FIFO along with the 1st byte of data and when this byte is transferred, the last byte flag selects the frame terminate register by asserting RS0 on the 6854. By this means, the transmitted frames are terminated without processor intervention. For sending short messages under processor control, a Multibus access to the address of a TX FIFO+1 will set the frame terminate flag with the stored byte of data. A short frame can then be sent without DMA control.

APPENDIX C

BINARY I/O CARD

The Binary I/O card is described in Controls Hardware Release No. 4.

APPENDIX E

FIBER OPTIC LINK REPEATER CHASSIS

E. 1 INTRODUCTION

The Link repeater chassis associated with each Linac Secondary station allows each secondary to receive data from and transmit data to the Primary station. The repeater is built as a separate chassis so that an individual station can be powered down without interfering with the rest of the communication loop.

E. 2 DESCRIPTION OF THE REPEATER CHASSIS

The repeater contains a receiver section, a logic section, and a transmitter section. The circuit diagram is given in Figure E. 2.

E. 2. 1 Receiver Section

Optical data is input to the Motorola MFOD404 photodetector module that is mounted in the chassis connector. This module contains the photodiode and an integral amplifier that outputs a differential signal to the MFOC600 receiver chip. Optical power input to the MFOD404 is converted to an electrical signal with a sensitivity of 30/mv/uw. This signal is converted to TTL by the MFOC600.

The incoming signal uses self clocking Manchester encoding. Clock and data information are separated and input to the logic section. A phase-locked loop (U7) serves to eleminate accummulated jitter in the detected clock signal.

E.2.2 The Logic Section

Most of the conventional logic for the repeater chassis is contained in U11, a 12L6 PAL (Programmable Logic Array). The PAL generates four output signals:

BYPASOUT - Causes this station to be bypassed.
TXCLK - Selects whether the received clock or the local clock is used to transmit.
TXDATA - Selects either the incoming data or the output data from this station to transmit.
RXENV - An envelope of the messages received on the link.

E.2.2.1 BYPASOUT -

A Secondary station may be bypassed to allow the rest of the link to operate while an individual system is offline. Four conditions will cause a bypass; 1)Loop Online Control requests the repeater chassis to bypass. This LOC line is operated by the 68000 and the MC6854 in a way that the station can go online and offline without interferring with messages on the link. The MC6854 transitions the LOC bit between messages. 2) A manual Bypass switch will force a bypass but the bypass occurs at the instant the switch is thrown. An error will be generated if a message is in progress. 3,4) If the secondary station power (5v) is turned off or if the ribbon cable connecting the link chassis and communication card is disconnected, the link will cause the station to be bypassed. An error may be generated.

When bypass is in effect, the decoded receive clock and data are output to the encoder circuitry and the fiber optic transmitter.

E.2.2.2 TXCLK -

TXCLK is the clock signal used by the transmitter section to encode the transmit data. Under both normal operating and bypass conditions TXCLK is the same as the RXCLK. Under some failure conditions, a local osillator is switched in and used as the TXCLK. The local clock is enabled by the RTS output from the MC6854, a pin operated by the 68000. The local clock frequency is 1.0MHz.

E.2.2.3 TXDATA -

TXDATA, the serial bit stream of data input to the transmit encoder, is usually the output data from the MC6854 SDLC chip. During BYPAS decoded receive data is sent directly to the transmitter by way of the PAL.

E.2.2.4 RXENV (Receive Data Envelope) -

In order to observe the incoming message traffic receive data envelope detector circuit is included in the link repeater chassis. This circuit determines if the incoming data is different from SDLC flags (01111110) and if a flag was detected within the past 40 ms. The first condition indicates that data is present while the second condition requires that the link is working.

E.2.3 Transmitter Section

The PAL outputs TXCLK and TXDATA are encoded into a self clocking Manchester signal using an exclusive OR and a dual latch (431 and 434). The combined signal is input to a 75450 driver that powers the fiberoptic transmitter, a Motorola MFOE106 Infra-Red emitter. A 500 ohm variable series resistor adjusts the amount of drive in order to control the optical output power. This power is normally set to about 10 db mw of optical power arriving at the next receiving station.

E.3 FRONT PANEL

The front panel of the fiber optic repeater chassis shown in Fig. 3.4.2 has a combination of LEDs and test points to aid in determining the status and operation of the link.

Each of the four Bypass conditions described in 2.2.1 is given a small yellow LED and the Bypass Status is shown by a large red LED.

Along the left side of the front panel is a group of LEDs and test points. Those are described below. All LEDs are tied to +5V and pulled low in the active state.

TX CLK ENABLE A yellow LED that is on when the local 1 MHz crystal oscillator is enabled by the processor. It is activated by the M6854 RTS pin. The test point is the low active side of the LED.

APPENDIX F

16-CHANNEL S/H-AD CHASSIS

F.1 INTRODUCTION

The majority of Linac analog signals are pulsed. Examples include beam current, RF parameters and drift tube quadrupole currents. Because of the pulsed nature of these signals, they must be sample and held before being digitized for input to the computer.

A small modular 16 channel chassis is used to house both that sample-and-hold circuit and the digitizer for a group of analog signals. Each station contains several of these chassis. The circuit diagram for this chassis is shown in Fig. F.1.

F.1.1 Description Of The Chassis

The SH/AD chassis receives analog input signals on two 8-pin coaxial connectors. Each channel is routed to a Harris 2425 sample-and-hold amplifier and the outputs of these amplifiers are input to a 16 channel multiplexed analog-to-digital converter (Analogic model 6812). The digitizer output is buffered onto a 50 conductor ribbon cable bus by way of a card edge connector at the rear of the chassis.

The buffers are tri-state devices so that all chassis may be daisy-chain connected. Channnel and chassis address data, a digitize strobe and output data are all carried on this bus. The entire group of chassis for a local station are driven by a three byte I/O connector included as part of a 9-byte binary I/O board in the local station.

In the three byte cable, two bytes are input and carry the twos complement left justified data from the digitizer. The third byte is output data to the chassis and the bit usage is defined as shown below:

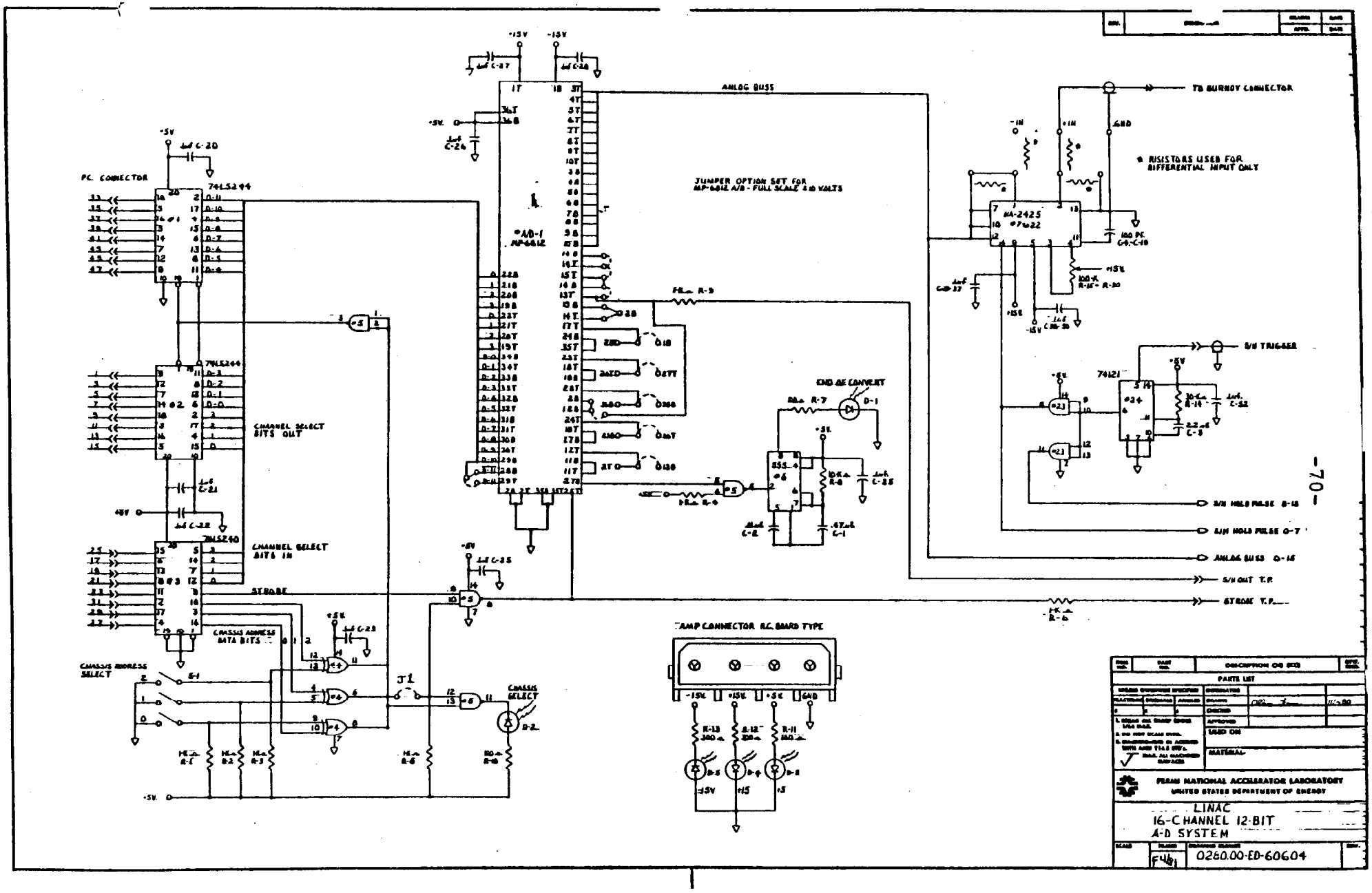
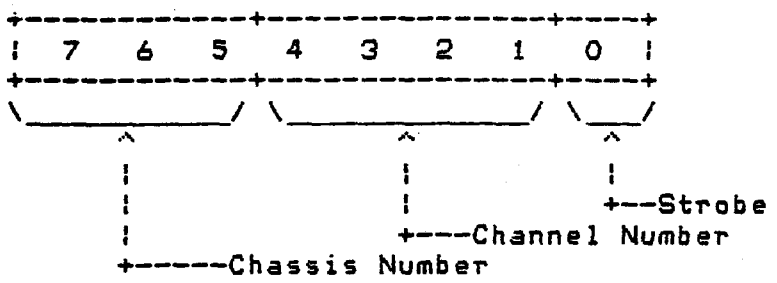


Figure F.1 Diagram of 16-Channel A/D Chassis



The digitize strobe is a 2 us high active strobe generated by the computer under program control. The chassis and channel number define a unique analog input channel and cause data from that channel to be output to the daisy-chained bus. When a digitize strobe occurs, the channel selected by the chassis/channel number will be digitized.

All digitizer chassis are set up to read +10V F.S. signals except chassis AD-0 is jumpered for +2.5V F.S. in order to obtain two more bits of resolution for RF power readings. These signals seldom exceed one volt.

F.2 JUMPER OPTIONS

Jumper connections for both the 10V and the 2.5V full scale ranges are provided. The jumper connections for the +10V version are indicated on the schematic drawing by dashed lines.

As installed, all of the Harris 2425 sample and hold circuits are operated as single-ended gain of one followers. The hold pulse is generated by a 40 ms one-shot triggered by sample and hold trigger input on the J3 BNC input connector on the rear panel.

Jumper J1 is removed so that the A.D digitizes the selected (1 of 16) channel each time a digitize strobe is generated. That is, the chassis number is not examined to determine if the selected channel number is located in a given chassis.

When operated in this mode, the computer can issue a single digitize strobe and then collect the result from each chassis in turn. This speeds up the reading process because the computer does not need to wait for the conversion time for each channel.

F.3 FRONT PANEL

There are no operator controls on front panel. Indicator LEDs are provided to show End-of-Convert, chassis select and +5, +15 power. convert strobe and the internal Sample-and-Hold output of 6812 digitizer module. The strobe test point will show the time at which the computer is gathering data and the S-H OUT test points shows the analog value of the selected channel during the digitize time. This test point is useful to determine if the digitizer is functioning properly.

F.4 REAR PANEL

The rear panel contains interface connectors J1 and J2 for the analog inputs, J3 for the S-H Trigger and the daisy-chained ribbon connector. The three-bit chassis number is set by way of a DIP switch accessable through the rear panel. Chassis numbers are normally chosen to begin at zero and count up for as many chassis as are installed.

H.3 WATCHDOG TIMER

A somewhat unrelated feature of the board is the system watchdog timer. This timer consists of a 220 ms retriggerable one shot that triggers a 100 us one-shot that provides a system reset on P2 pin 38. After system initialization the 68000 performs a write to address $6118 to trigger the 220 ms one-shot. This is done each Linac cycle by a task that is triggered during the 15 Hz interrupt. The timer is retriggered each cycle but for any reason if the processor does not trigger the one-shot for three cycles, the watchdog timer will time out and trigger the second one-shot that generates a system reset. One and only one reset pulse is generated, but under normal circumstances this reset will restart the system. This feature is enabled by a toggle switch on the front edge of the board. A cut trace option will disconnect the signal from P2.

H.4 PREDET TIMERS

Three Motorola MC6840 chips provide the counters used in the predet channels. Delay times are loaded into these chips during system initialization. The timers are configured to count the E clock and a trigger input normally starts all timers simultaneously. Once a timer is triggered it counts for a time determined by the number in the preload register, and then the output transitions from high to low. This trailing edge is used to trigger a one shot that outputs a 1 us pulse which is buffered with a 75452 and transformer coupled off the board. A power on inhibit circuit disallows any output pulses during a power-up sequence.

Although the board is designed to make each timer independent, cut trace options and jumpers points are provided to allow one timer to be triggered by the timeout of another timer. These jumpers are grouped near each 6840 and are organized to allow one timer output to trigger either of the other timers within the chip. This is useful to generate pulse-on/pulse-width functions.

H.5 TIME BASE INPUT

The timer board is designed to expect a 1 MHz input time signal that is normally the Booster clock. This signal is input to a NE564 phase locked loop with a divide by two in the feedback loop to generate a 2 MHz clock at the phase locked loop output. If the input 1 MHz signal is removed, the phase locked loop continues to operate, but at a slightly different frequency. Only a few tens of millivolts